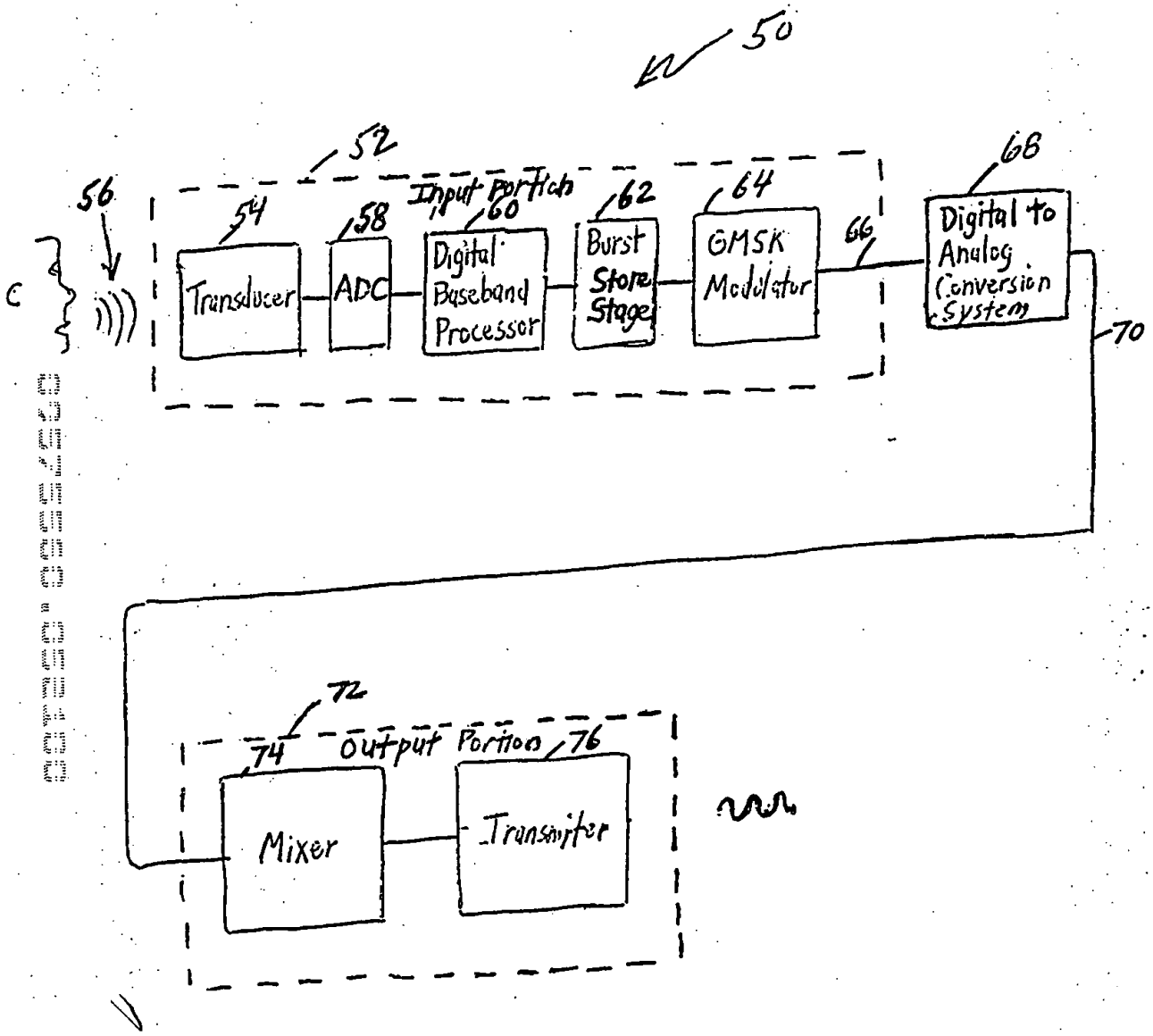

50
52
Input Portion
56
54
58
60
62
64
66
68
70
C
Transducer
ADC
Digital Baseband Processor
Burst Store Stage
GMSK Modulator
Digital to Analog Conversion System
72
74
Output Portion
76
Mixer
Transmitter

FIG. 1

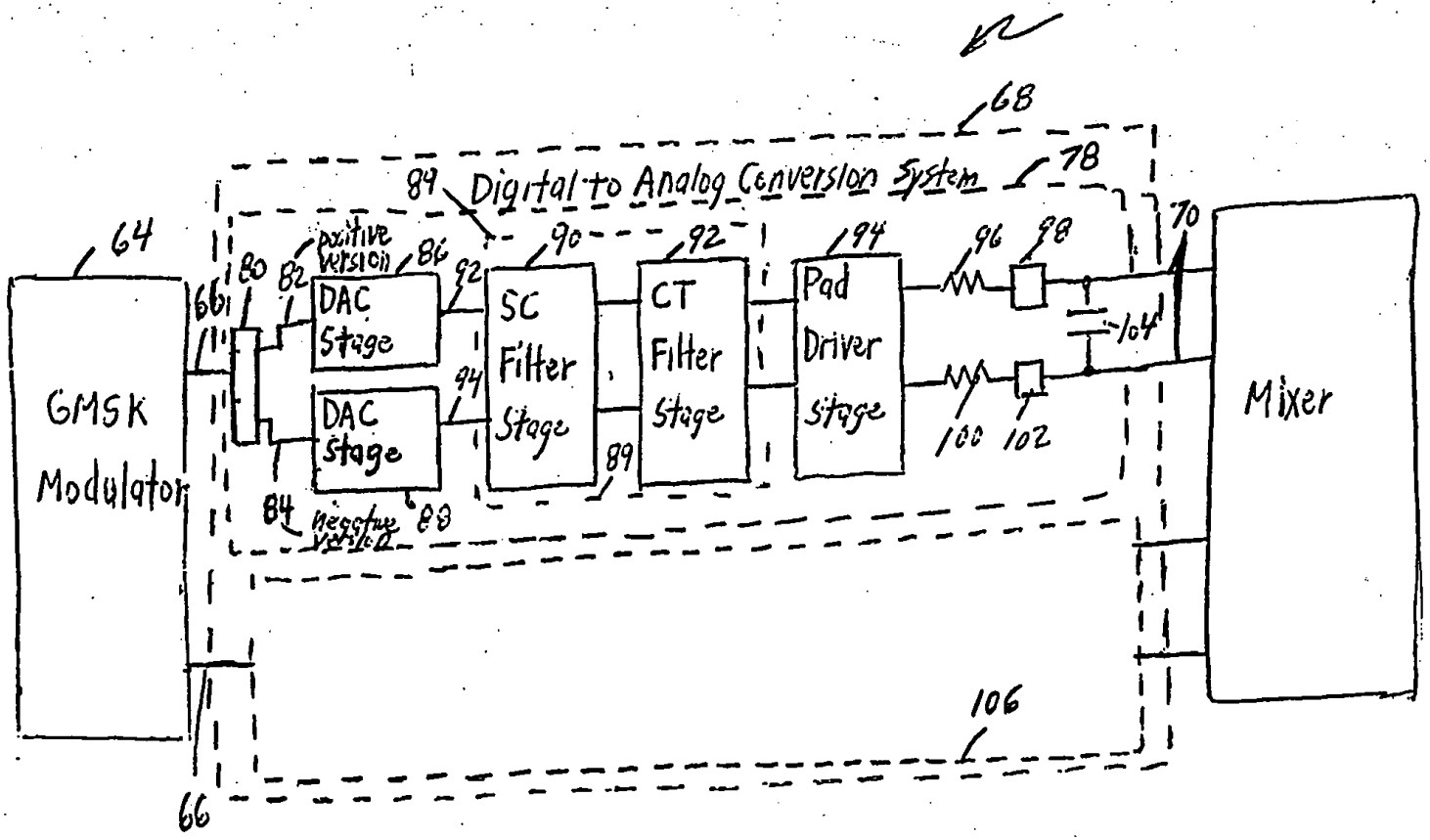

68
Digital to Analog Conversion System
78
64
GMSK Modulator
66
positive version
DAC Stage
DAC Stage
negative version
SC Filter Stage
CT Filter Stage
Pad Driver stage
Mixer
70
104
106
80
82
84
86
88
89
90
92
94
96
98
100
102

FIG. 2

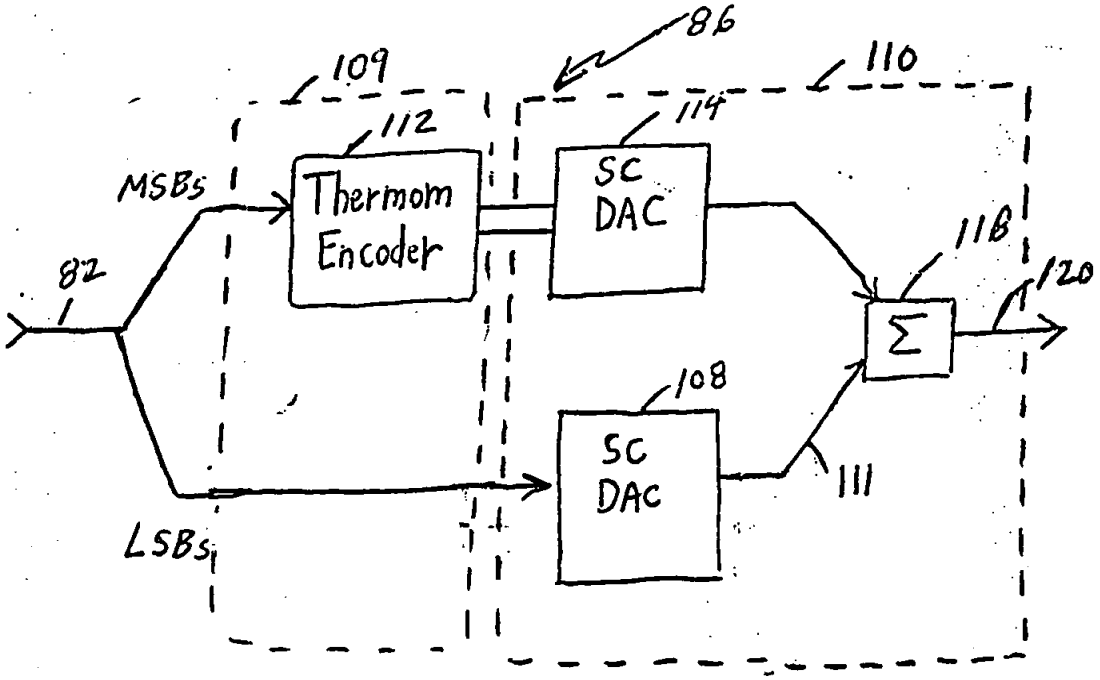

86
109
110
112
114
MSBs
Thermom Encoder
SC DAC
82
116
120
Σ
108
SC DAC
111
LSBs

FIG. 3

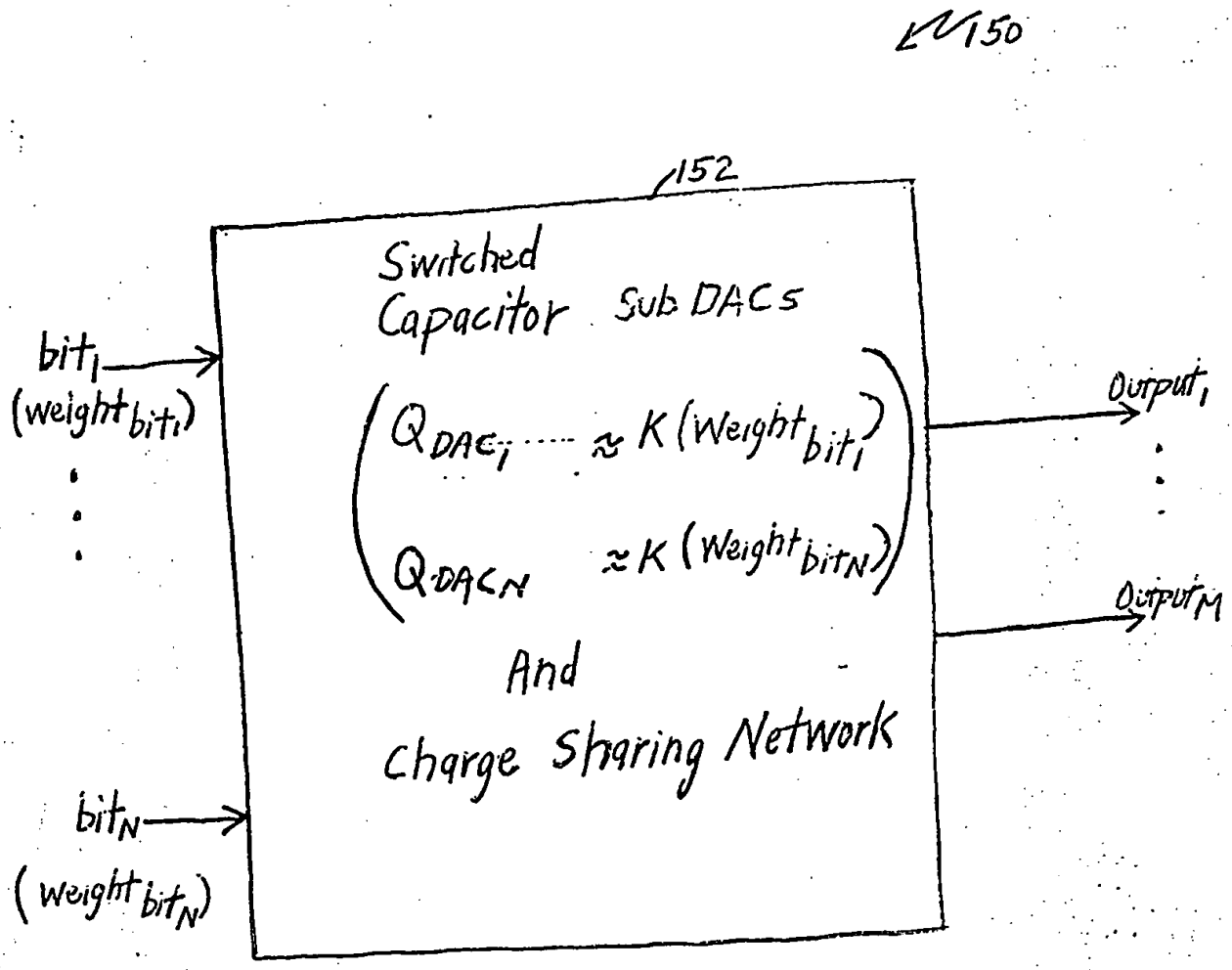

150
152
Switched
Capacitor Sub DACs
$bit_1$
$(weight_{bit_1})$
$bit_N$
$(weight_{bit_N})$
$Q_{DAC_1} \approx K(Weight_{bit_1})$
$Q_{DAC_N} \approx K(Weight_{bit_N})$
And
Charge Sharing Network
$Output_1$
$Output_M$

FIG. 4

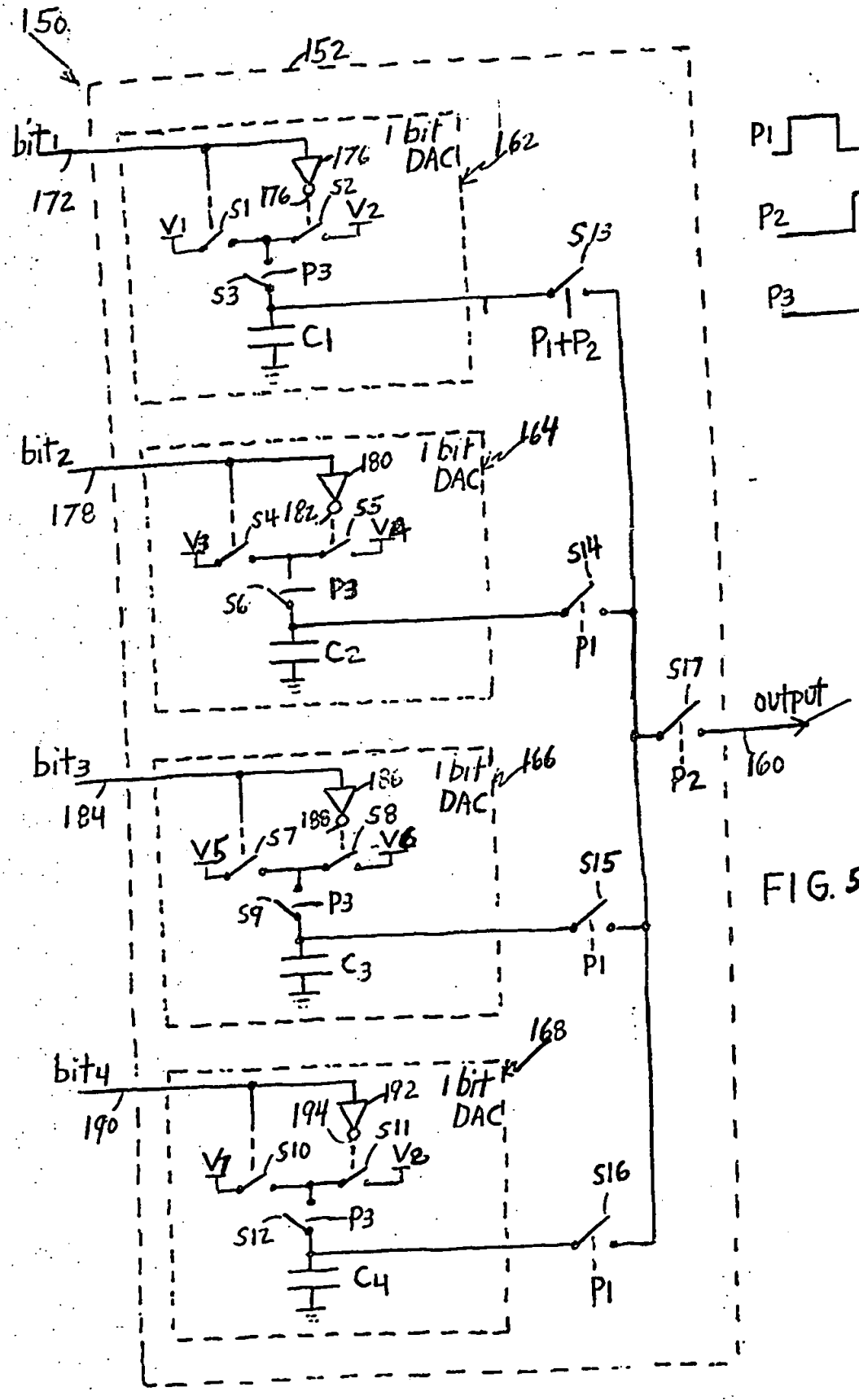

150
152
bit1
1 bit DAC
162
172
176
S1
S2
V1
V2
P3
S3
C1
S13
P1+P2
bit2
1 bit DAC
164
178
180
182
S4
S5
V3
V4
P3
S6
C2
S14
P1
bit3
1 bit DAC
166
184
186
S7
S8
V5
V6
P3
S9
C3
S15
P1
bit4
1 bit DAC
168
190
192
194
S10
S11
V1
V2
P3
S12
C4
S16
P1
S17
output
P2
160

FIG. 5

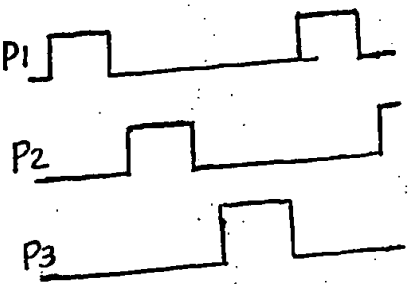

P1
P2
P3

FIG. 6

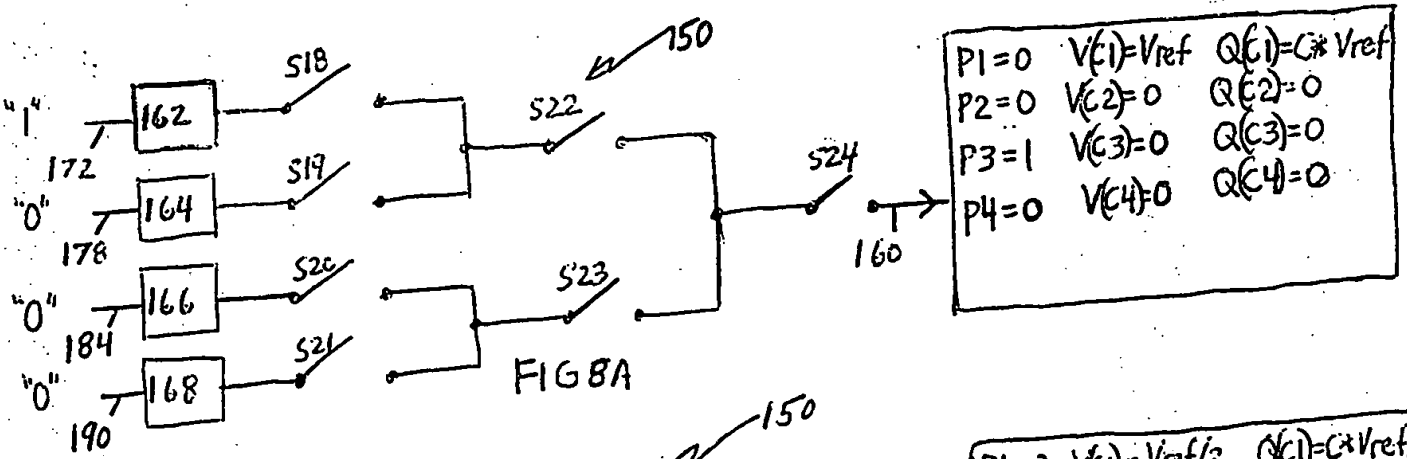



FIG 8A

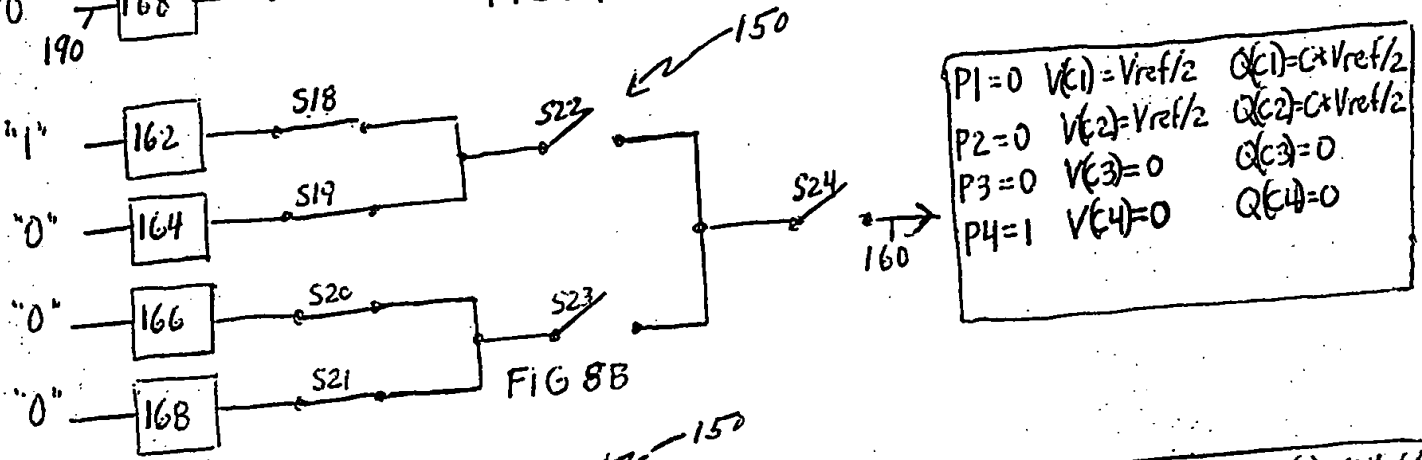



FIG 8B

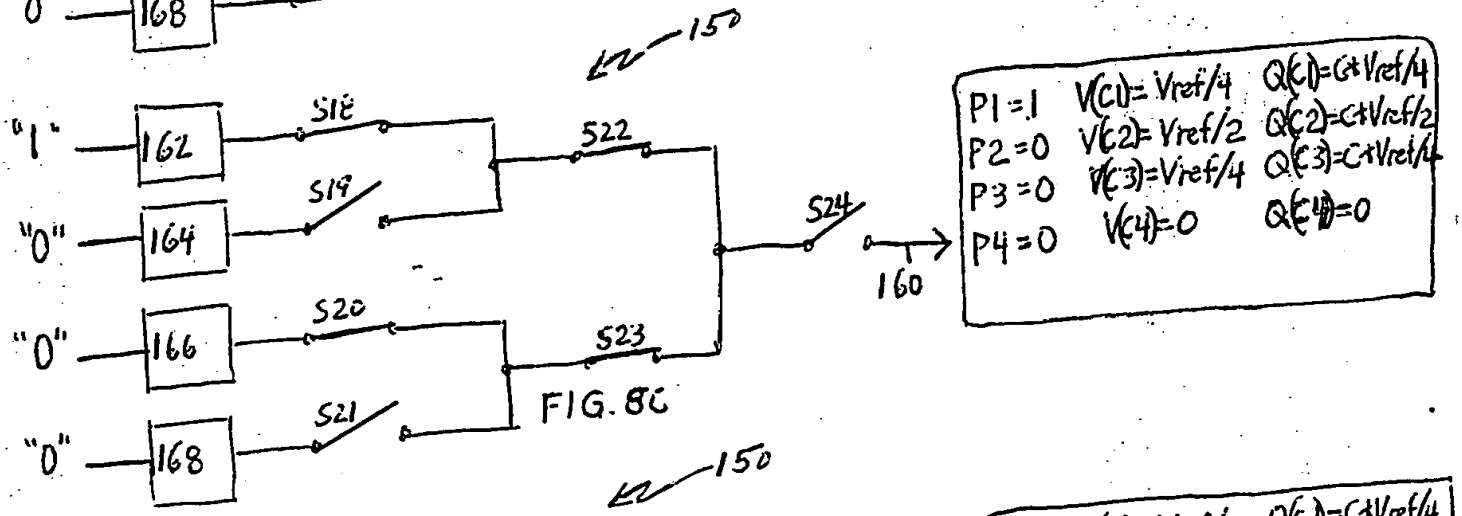



FIG. 8C

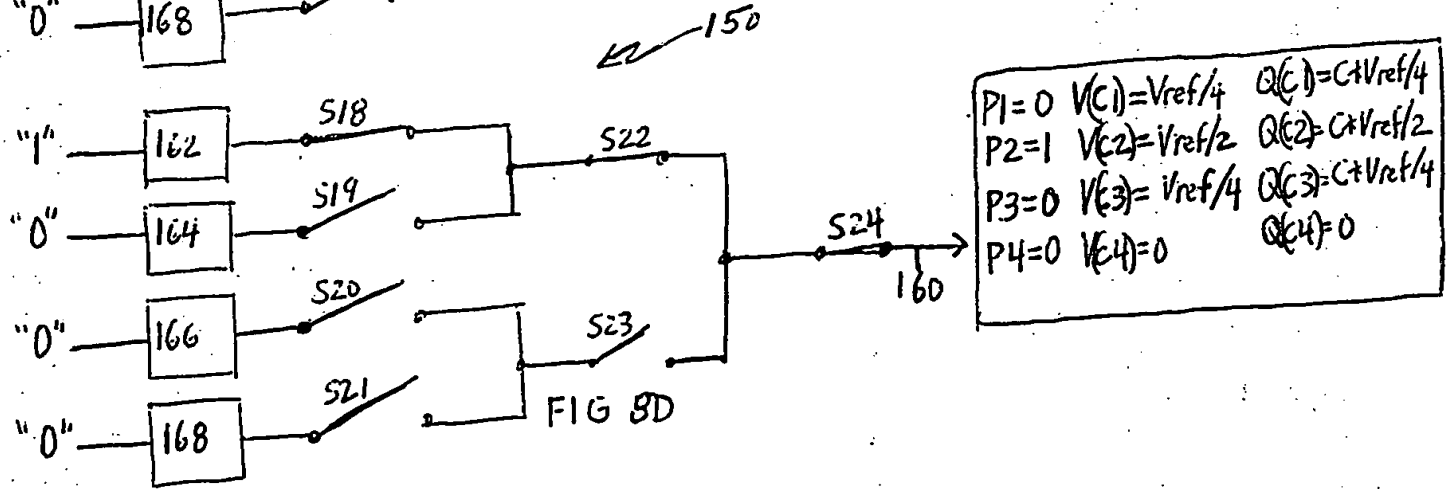



FIG 8D

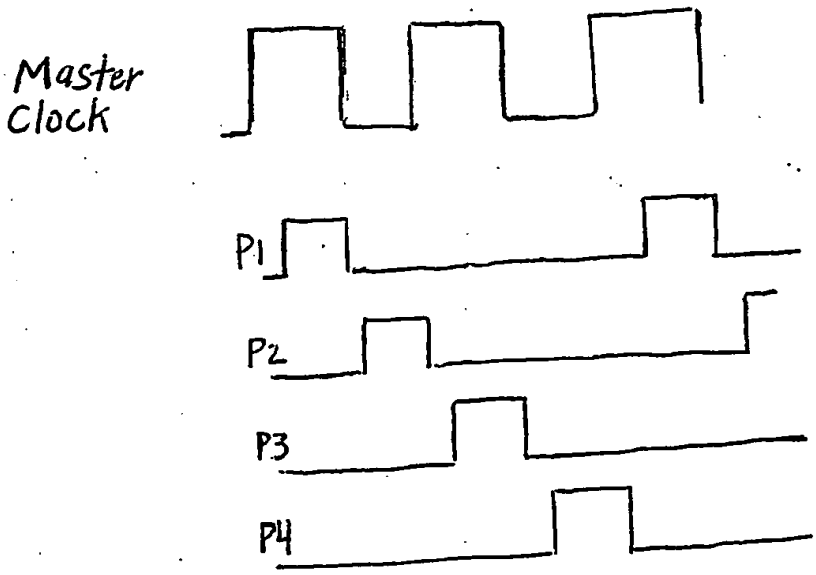



FIG 9

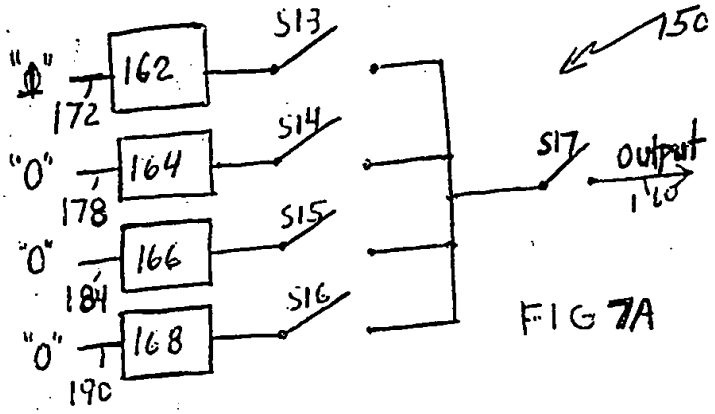



FIG 7A

| | | |
|---|---|---|
| P1 "0" | V(C1) = Vref | Q(C1) = C*Vref |
| P2 "0" | V(C2) = 0 | Q(C2) = 0 |
| P3 "1" | V(C3) = 0 | Q(C3) = 0 |
| | V(C4) = 0 | Q(C4) = 0 |

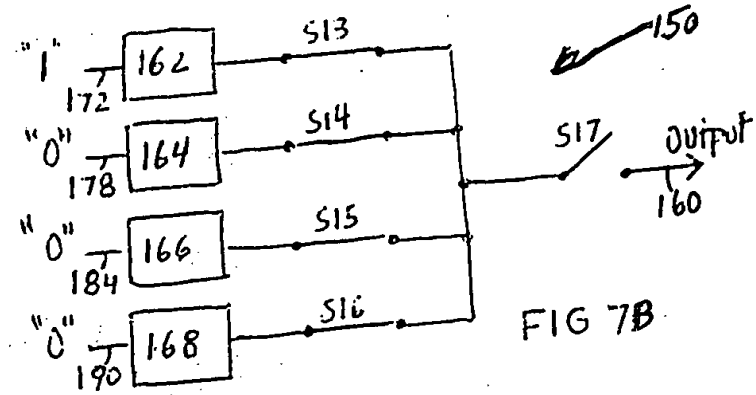



FIG 7B

| | | |
|---|---|---|
| P1 = "1" | V(C1) = Vref/4 | Q(C1) = C*Vref/4 |
| P2 = "0" | V(C2) = Vref/4 | Q(C2) = C*Vref/4 |
| P3 = "0" | V(C3) = Vref/4 | Q(C3) = C*Vref/4 |
| | V(C4) = Vref/4 | Q(C4) = C*Vref/4 |

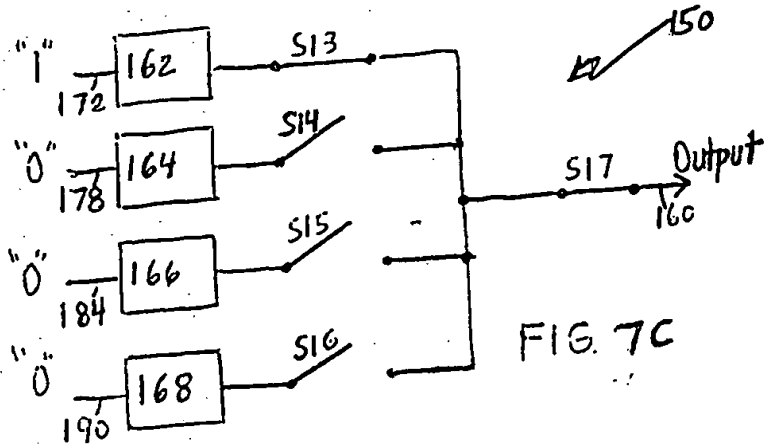



FIG. 7C

| | | |
|---|---|---|
| P1 = "0" | V(C1) = Vref/4 | Q(C1) = C*Vref/4 |
| P2 = "1" | V(C2) = Vref/4 | Q(C2) = C*Vref/4 |
| P3 = "0" | V(C3) = Vref/4 | Q(C3) = C*Vref/4 |
| | V(C4) = Vref/4 | Q(C4) = C*Vref/4 |

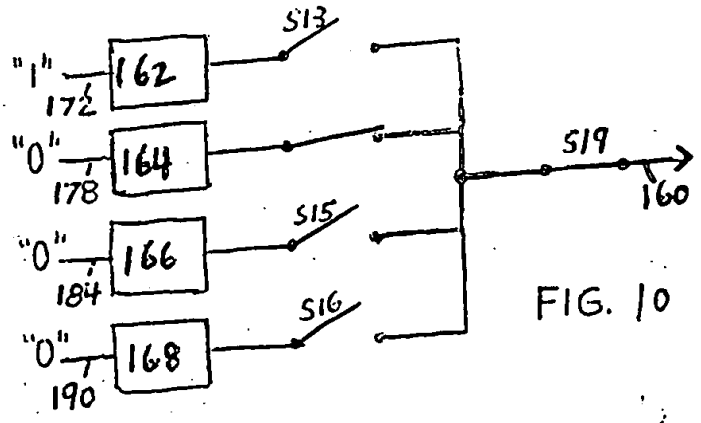



FIG. 10

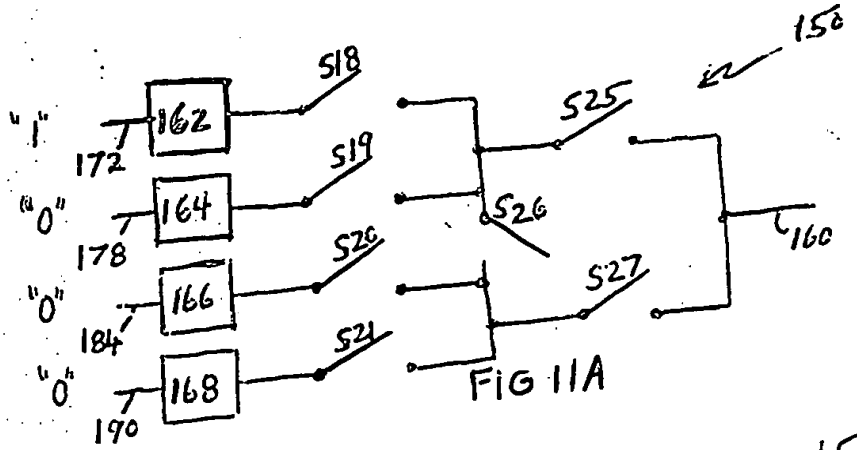



FIG 11A

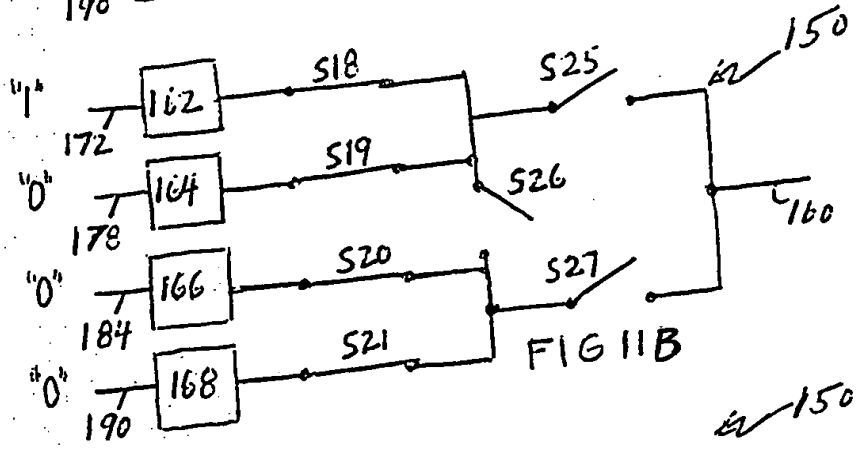



FIG 11B

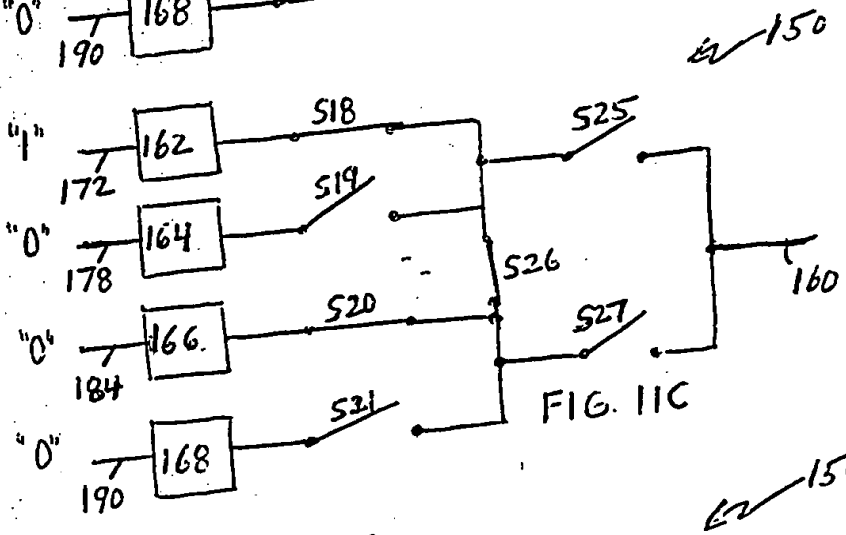



FIG. 11C

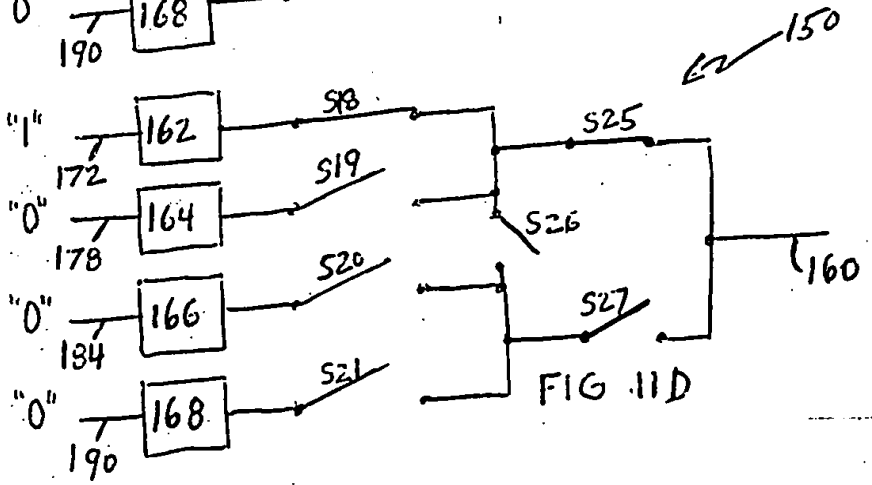
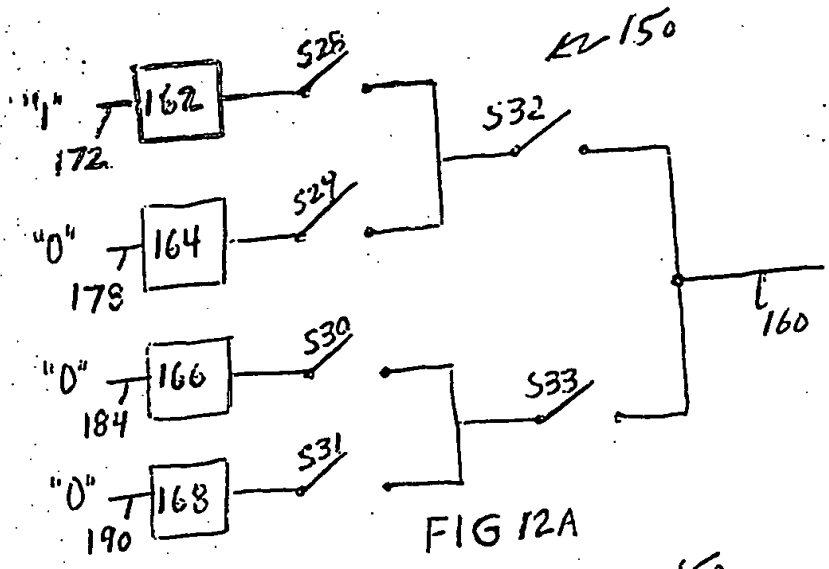
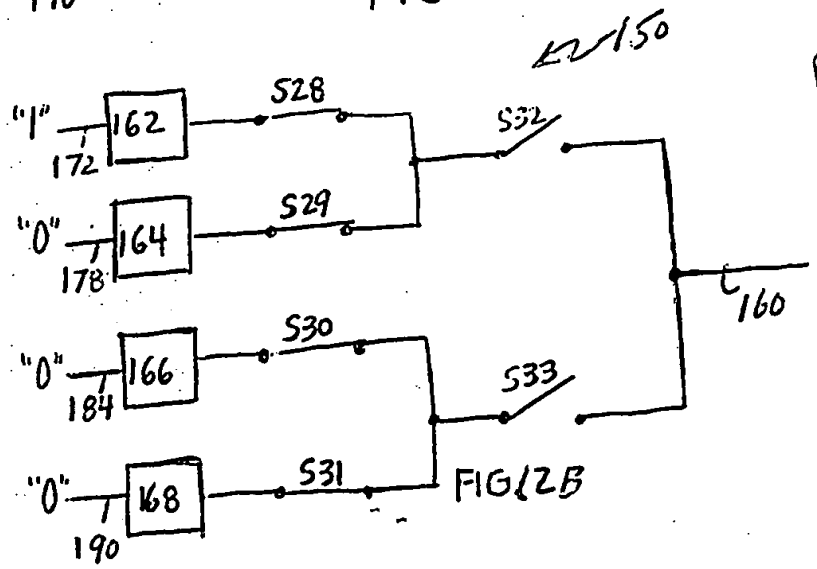



FIG 11D



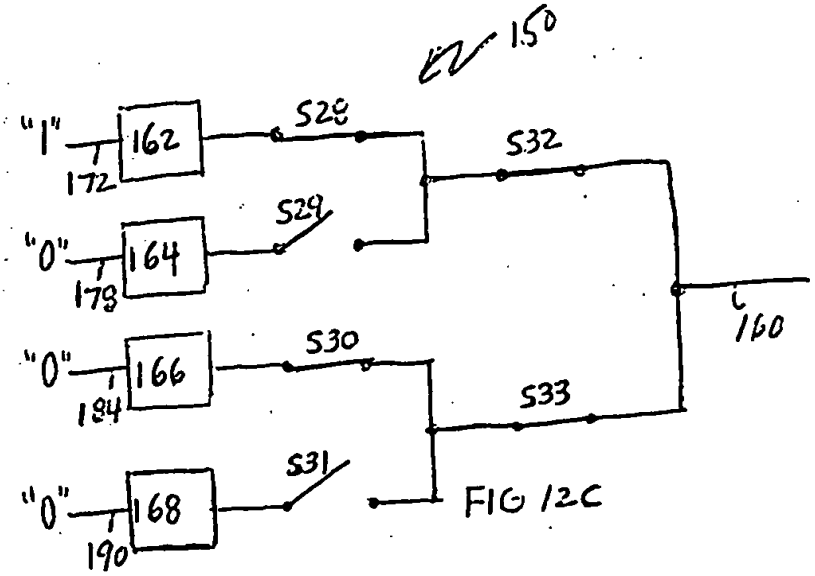

| | | |
|---|---|---|
| P1 = 0 | V(C1) = Vref | Q(C1) = C * Vref |
| P2 = 0 | V(C2) = 0 | Q(C2) = 0 |
| P3 = 1 | V(C3) = 0 | Q(C3) = 0 |
| | V(C4) = 0 | Q(C4) = 0 |

FIG 12A




| | | |
|---|---|---|
| P1 = 1 | V(C1) = Vref/2 | Q(C1) = C * Vref/2 |
| P2 = 0 | V(C2) = Vref/2 | Q(C2) = C * Vref/2 |
| P3 = 0 | V(C3) = 0 | Q(C3) = 0 |
| | V(C4) = 0 | Q(C4) = 0 |

FIG 12B




| | | |
|---|---|---|
| P1 = 0 | V(C1) = Vref/2 | Q(C1) = C * Vref/2 |
| P2 = 1 | V(C2) = Vref/2 | Q(C2) = C * Vref/2 |
| P3 = 0 | V(C3) = 0 | Q(C3) = 0 |
| | V(C4) = 0 | Q(C4) = 0 |

FIG 12C

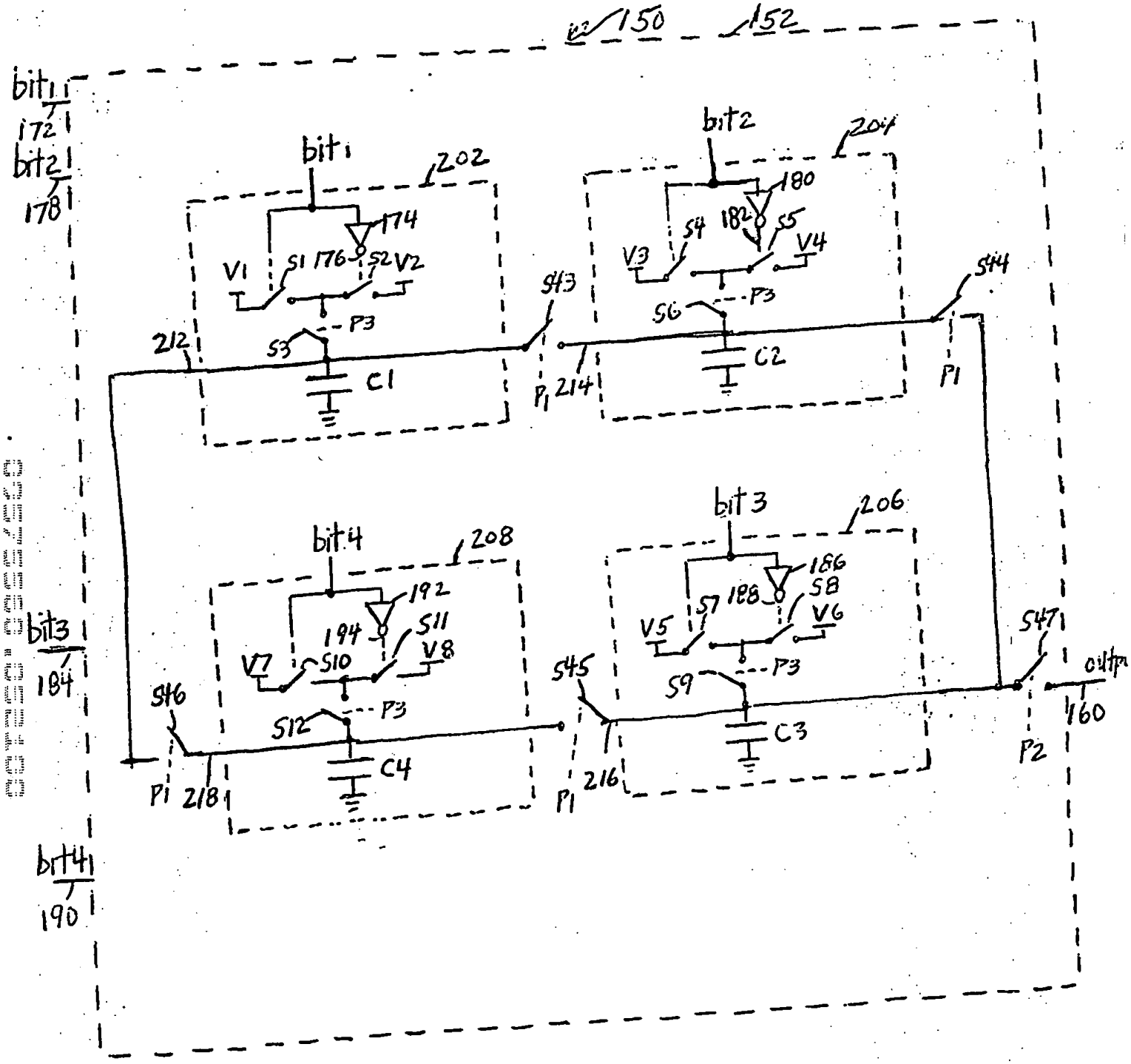
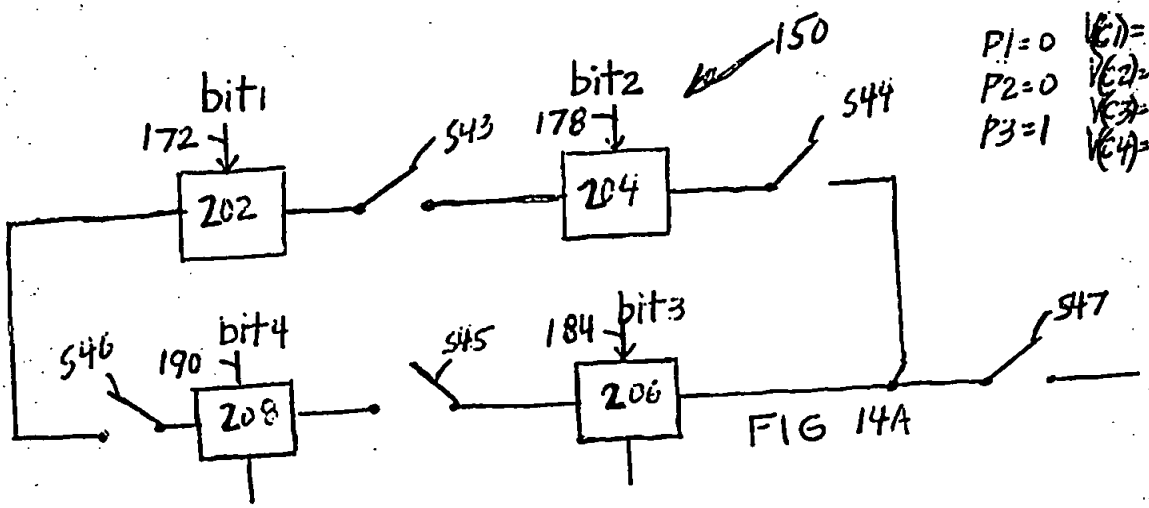
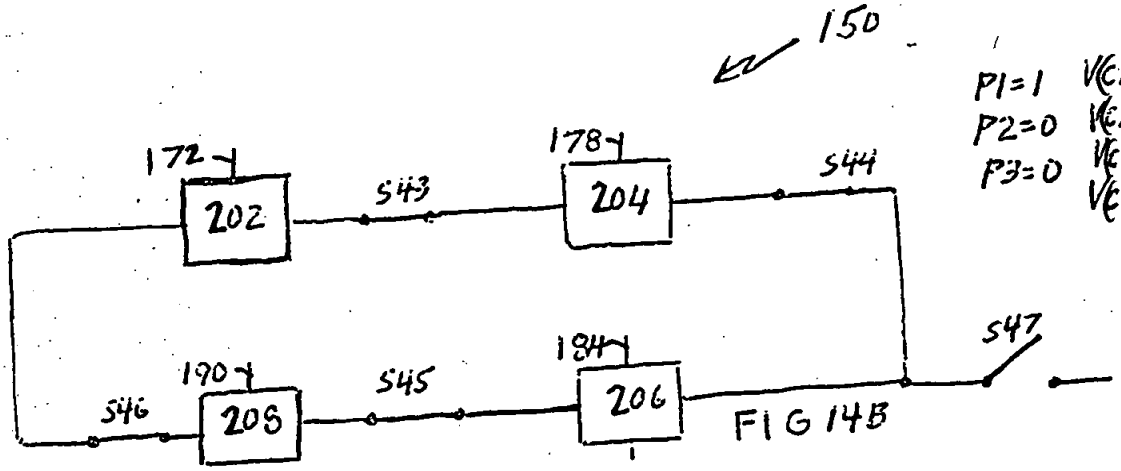

150
152
bit1
172
bit2
178
bit3
184
bit4
190
bit1
202
bit2
204
bit3
206
bit4
208
V1
S1
176
174
S2
V2
S3
P3
C1
212
S43
P1
214
V3
S4
182
180
S5
V4
S56
C2
S44
P1
V7
S10
194
192
S11
V8
S12
C4
S46
P1
218
V5
S7
188
186
S8
V6
S59
C3
S45
216
P1
S47
P2
outp
160

FIG. 13



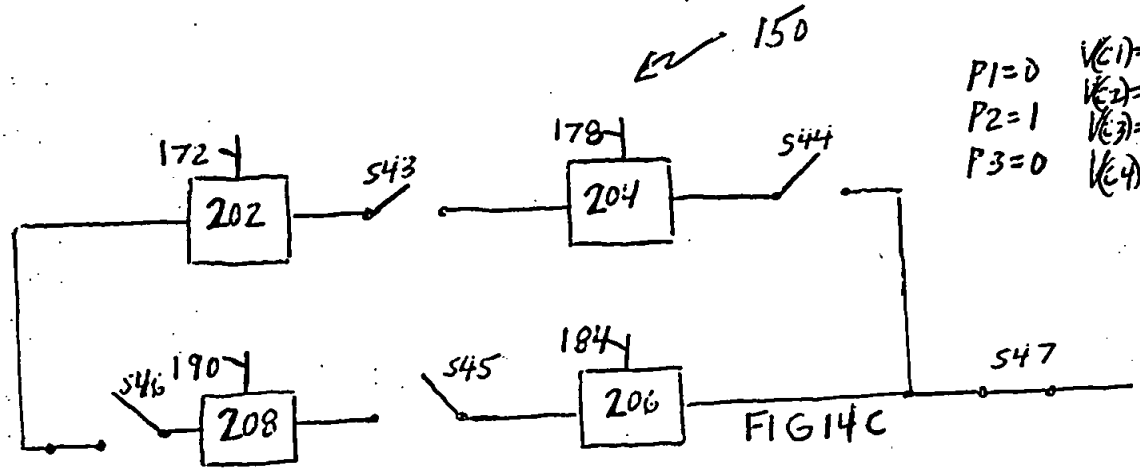

P1=0 V(C1)=Vref Q(C1)=C*Vref
P2=0 V(C2)=0 Q(C2)=0
P3=1 V(C3)=0 Q(C3)=0
V(C4)=0 Q(C4)=0

FIG 14A




P1=1 V(C1)=Vref/4 Q(C1)=C*Vref/4
P2=0 V(C2)=Vref/4 Q(C2)=C*Vref/4
P3=0 V(C3)=Vref/4 Q(C3)=C*Vref/4
V(C4)=Vref/4 Q(C4)=C*Vref/4

FIG 14B




P1=0 V(C1)=Vref/4 Q(C1)=C*Vref/4
P2=1 V(C2)=Vref/4 Q(C2)=C*Vref/4
P3=0 V(C3)=Vref/4 Q(C3)=C*Vref/4
V(C4)=Vref/4 Q(C4)=C*Vref/4

FIG 14C

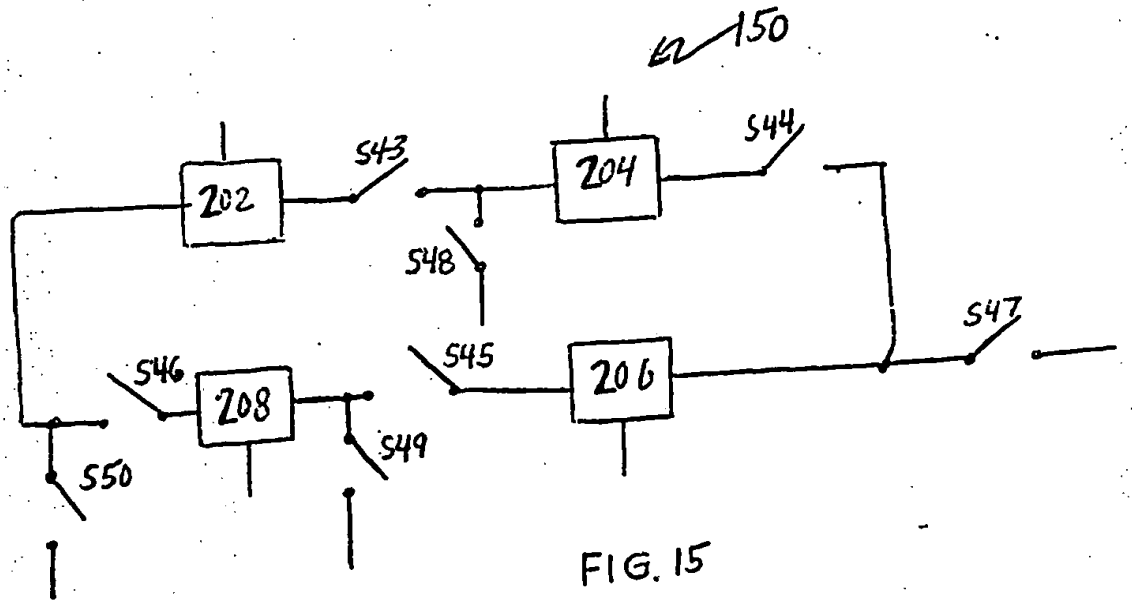



FIG. 15

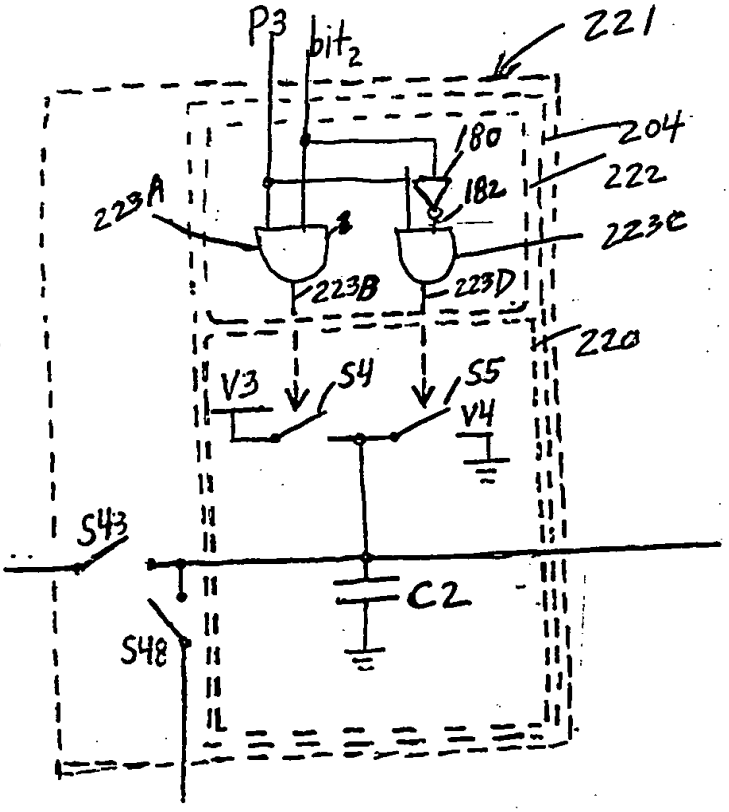



FIG16A

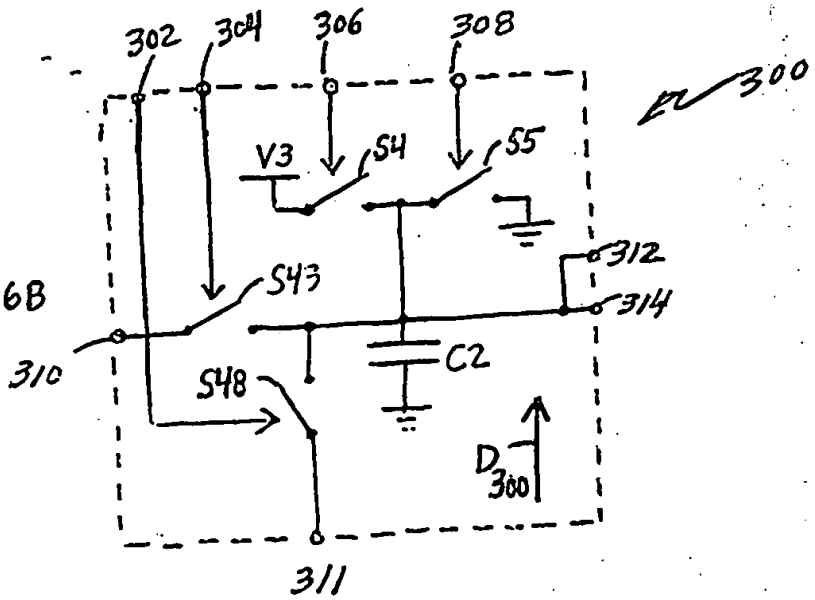



FIG16B

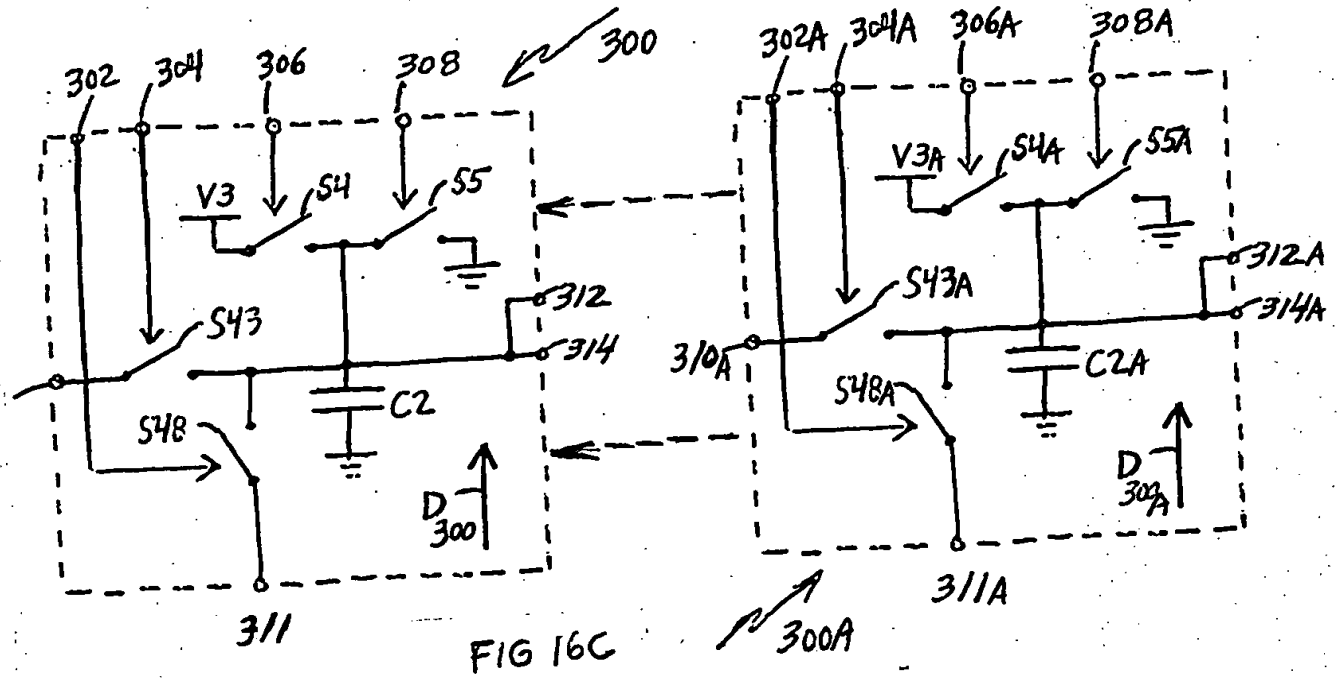



FIG 16C

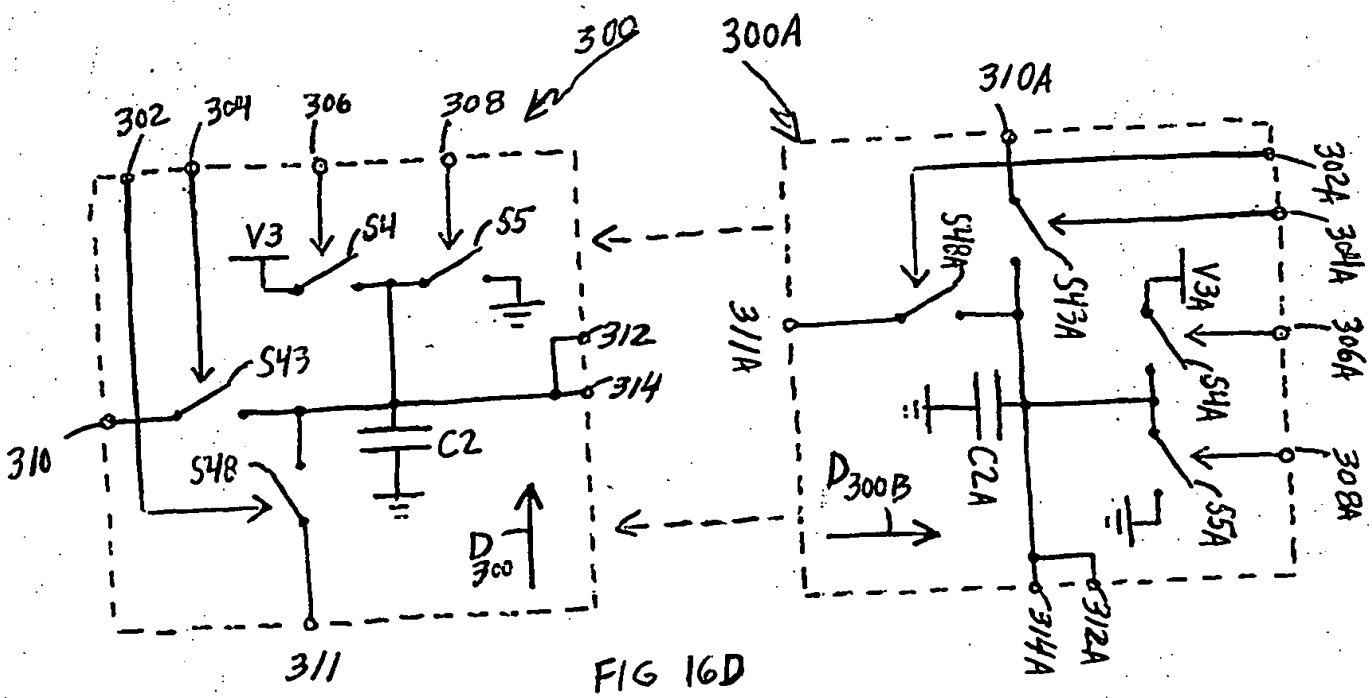
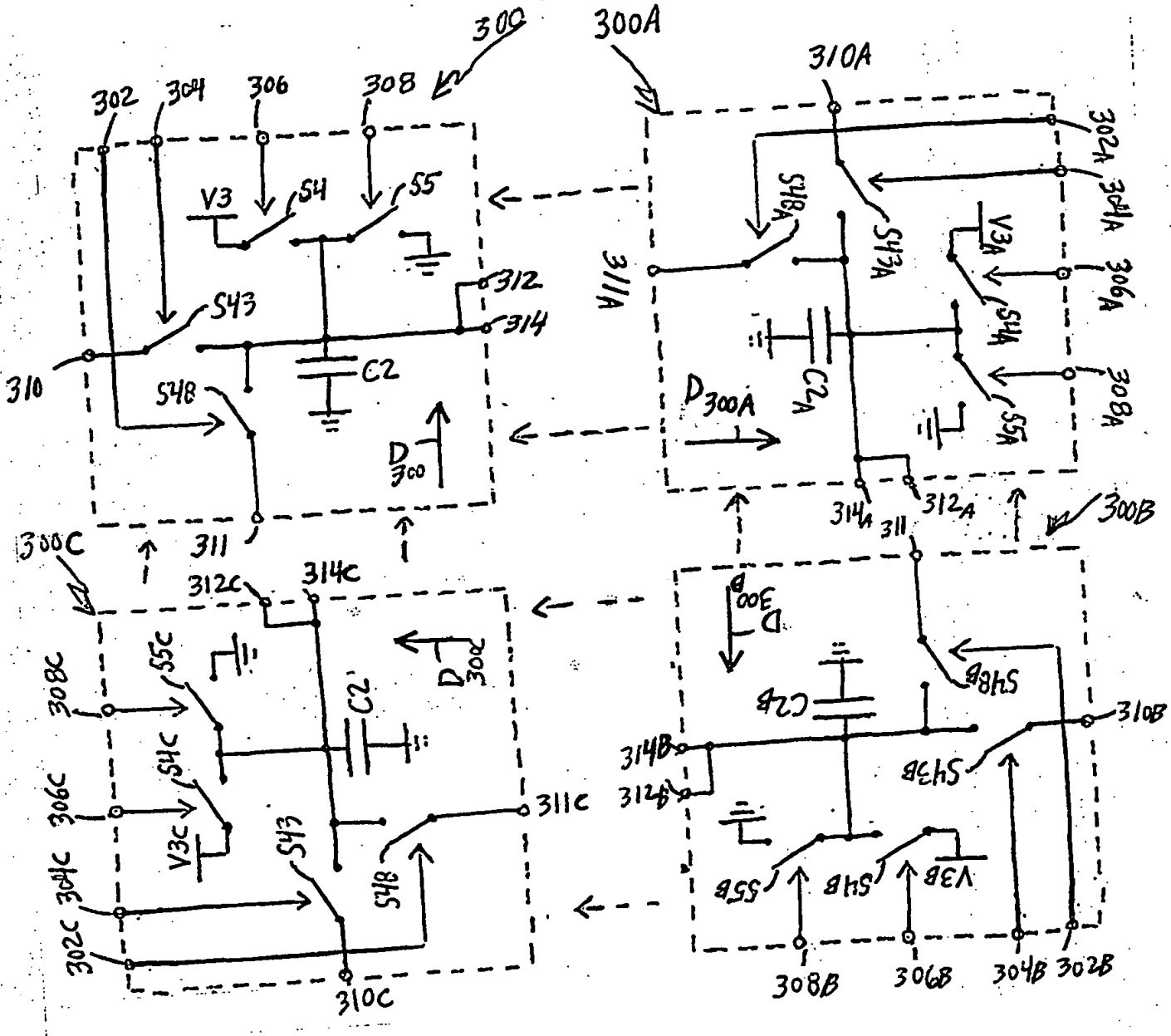



FIG 16D


300
300A
310A
302
304
306
308
V3
S4
S5
S43
S48
312
314
310
C2
311
$D_{300}$
$D_{300A}$
$C2_A$
$S48_A$
$S43_A$
$V3_A$
$S4_A$
$S5_A$
$302_A$
$304_A$
$306_A$
$308_A$
$314_A$
$312_A$
311A
300B
300C
312C
314C
308C
S5C
C2'
S4C
306C
V3C
S43
S48
311C
302C
304C
310C
$D_{300B}$
$D_{300C}$
C2B
$S48_B$
$S43_B$
$S4_B$
$S5_B$
$V3_B$
314B
312B
310B
308B
306B
304B
302B

16E

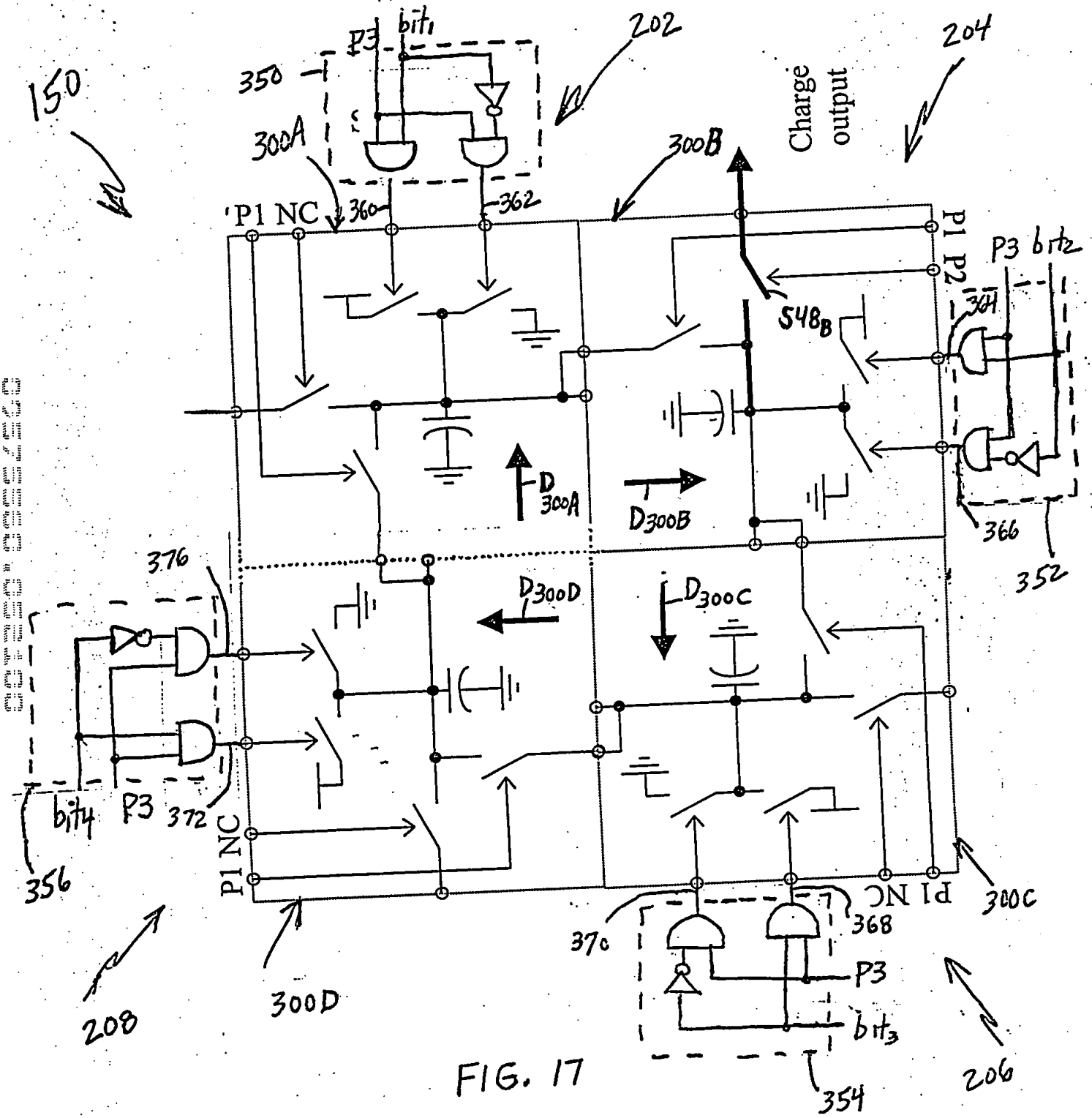

150
202
204
P3
bit1
350
300A
300B
Charge output
P1 NC
360
362
P1 P2
P3 bit2
361
S48B
D300A
D300B
366
352
376
D300D
D300C
bit4
P3
372
356
P1 NC
P1 NC
300C
370
368
P3
bit3
354
208
300D
206

FIG. 17

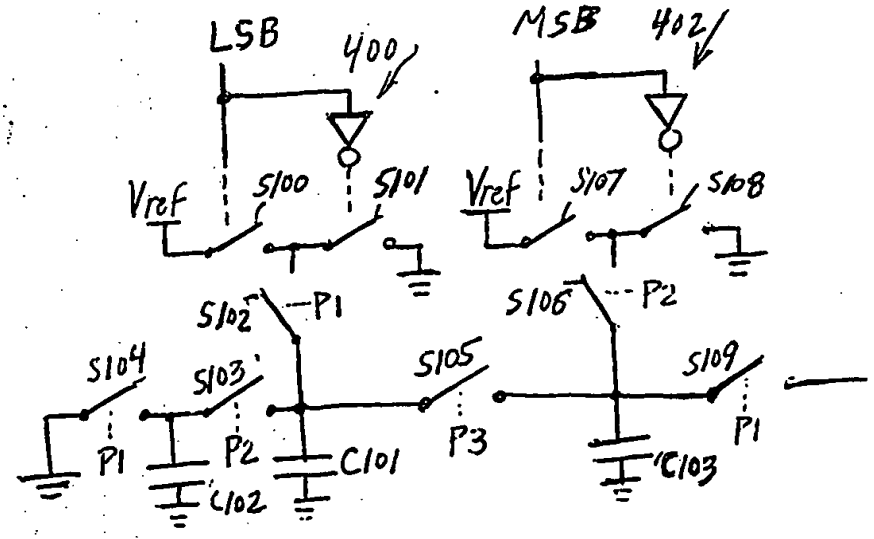
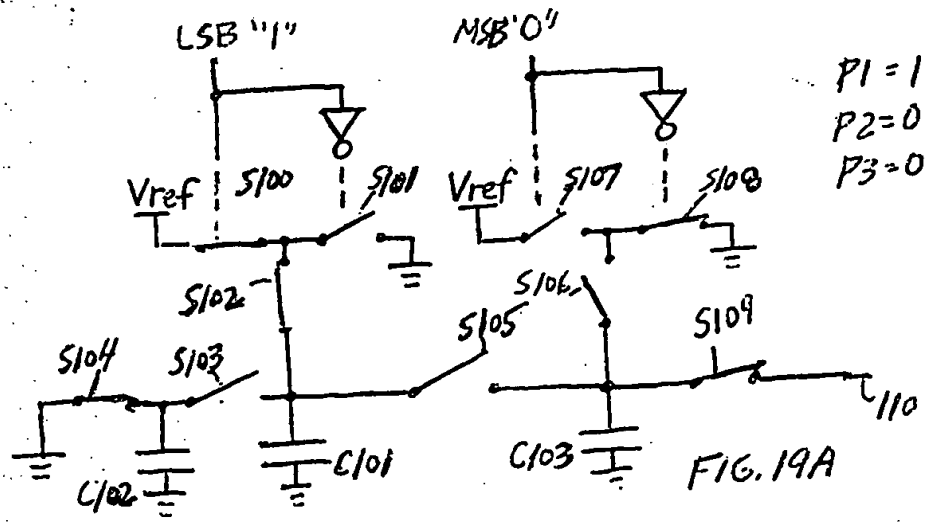
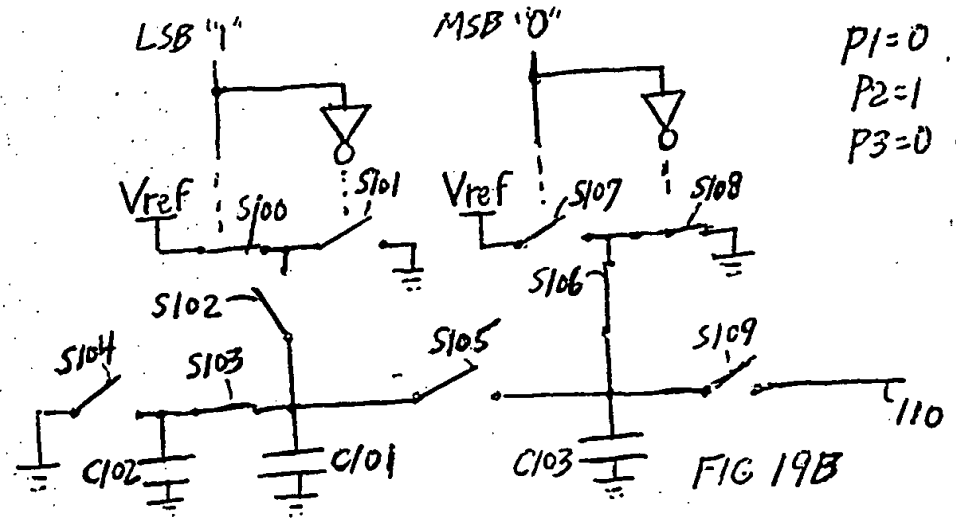

LSB
400
MSB
402
108
Vref
S100
S101
Vref
S107
S108
S102
P1
S106
P2
S104
S103
S105
S109
P1
P2
P3
P1
C101
C102
C103

FIG. 18



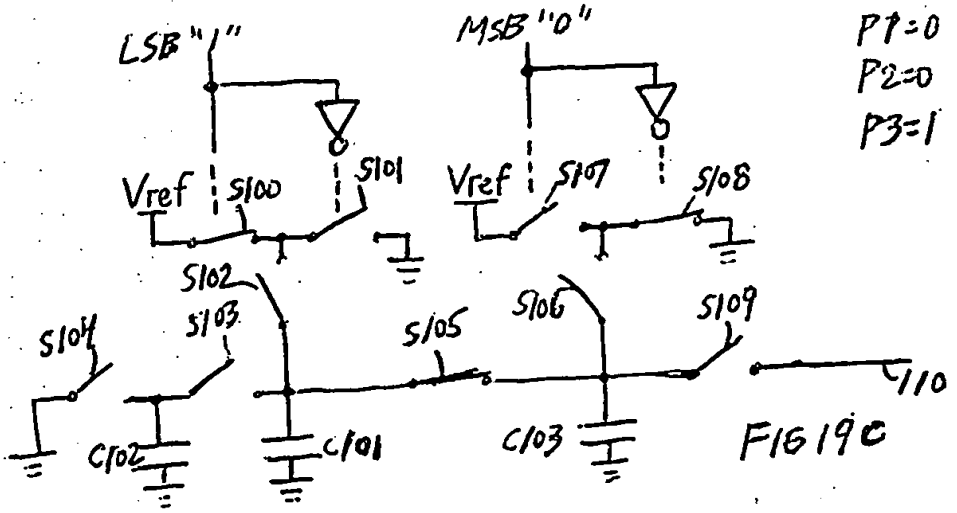

P1 = 1 V(C102) = 0 Q(C102) = 0
P2 = 0 V(C101) = Vref Q(C101) = C*Vref
P3 = 0 V(C103) = ? Q(C103) = ?

FIG. 19A




P1 = 0 V(C102) = Vref/2 Q(C102) = C*Vref/2
P2 = 1 V(C101) = Vref/2 Q(C101) = C*Vref/2
P3 = 0 V(C103) = 0 Q(C103) = 0

FIG 19B




P1 = 0 V(C102) = Vref/2 Q(C102) = C*Vref/2
P2 = 0 V(C101) = Vref/4 Q(C101) = C*Vref/4
P3 = 1 V(C103) = Vref/4 Q(C103) = C*Vref/4

FIG 19C

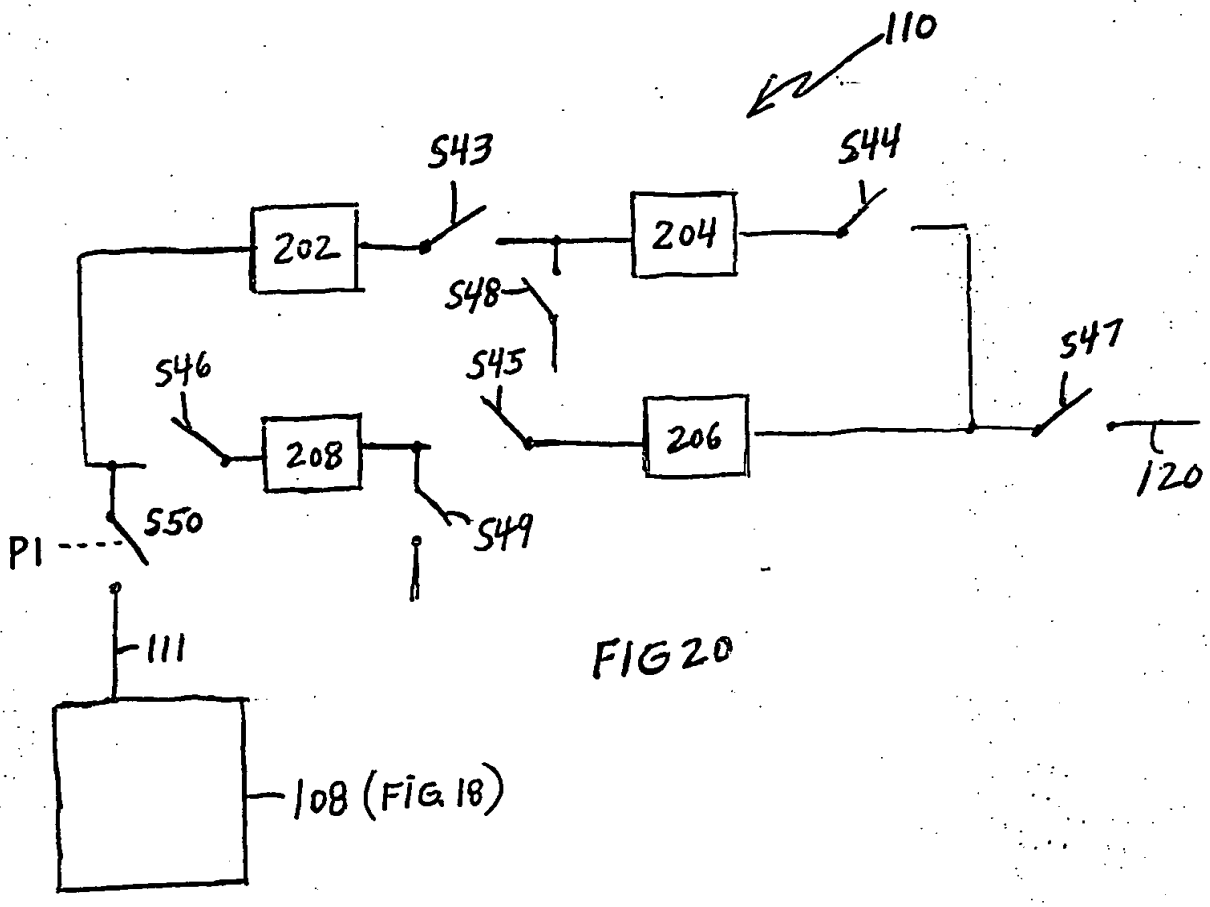

110
543
544
202
204
548
545
547
546
206
208
120
550
549
P1
111
108 (FIG 18)

FIG 20

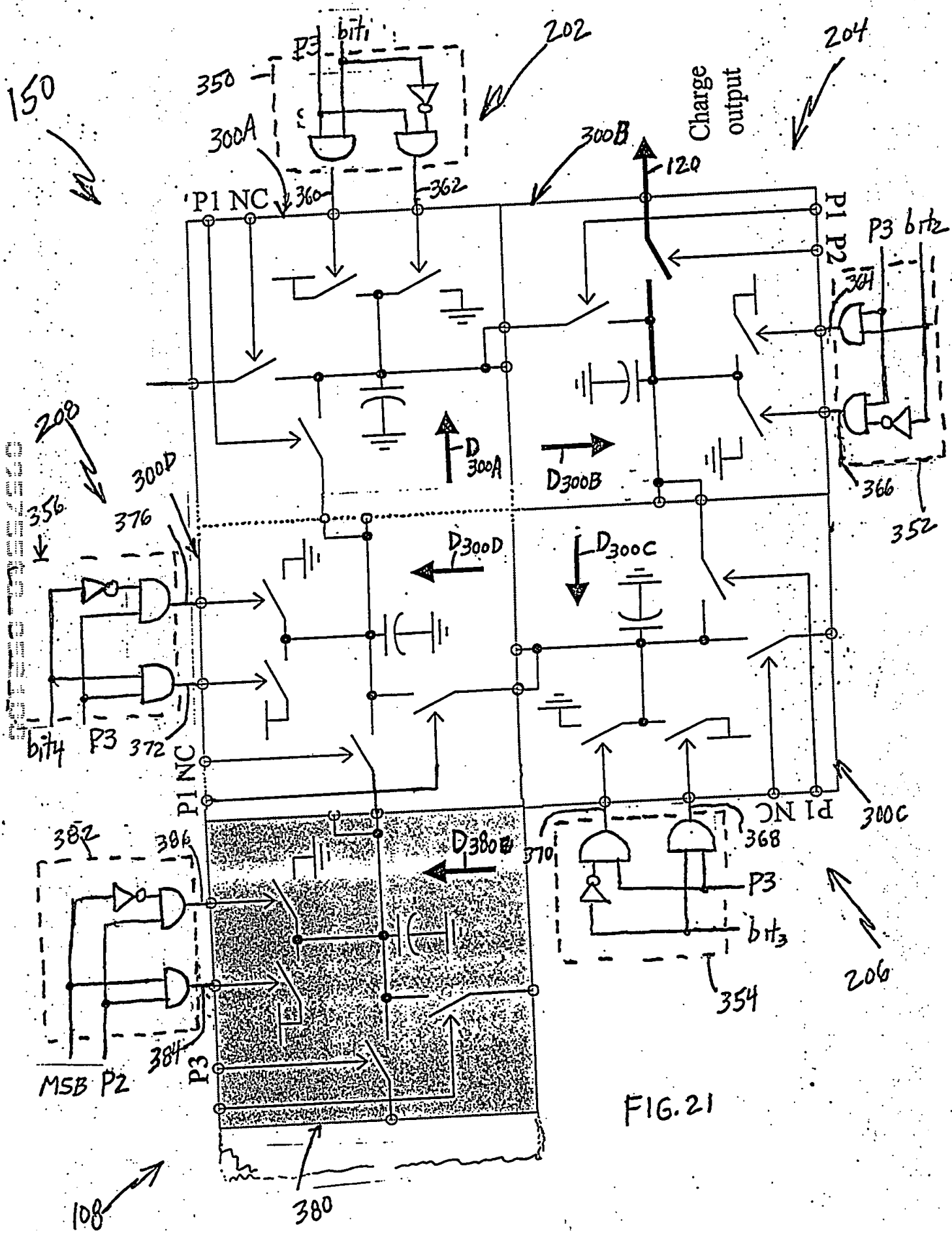

150
202
204
350
P3
bit1
300A
300B
Charge output
120
P1 NC
360
362
P1 P2
P3 bit2
364
208
300D
376
356
D300A
D300B
366
352
D300D
D300C
bit4
P3
372
P1 NC
P1 NC
300C
382
386
D380A
370
368
P3
bit3
354
206
384
P3
MSB P2
380
108

FIG. 21

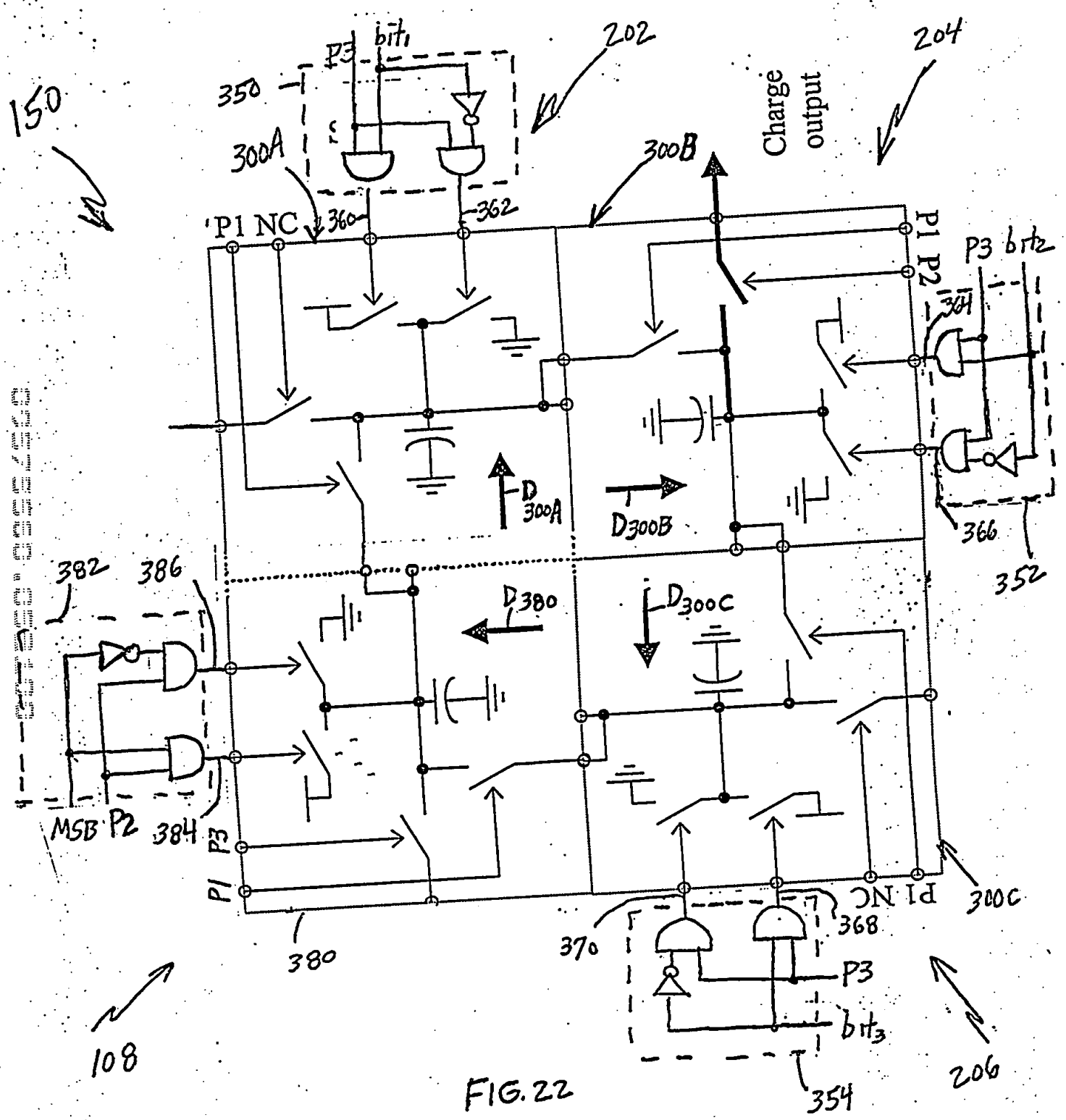

150
202
204
350
P3
bit1
300A
300B
Charge output
P1 NC
360
362
P1 P2
P3 bit2
364
366
352
D300A
D300B
382
386
D380
D300C
MSB P2
384
P3
P1
380
370
368
P1 NC
300C
P3
bit3
354
206
108

FIG. 22

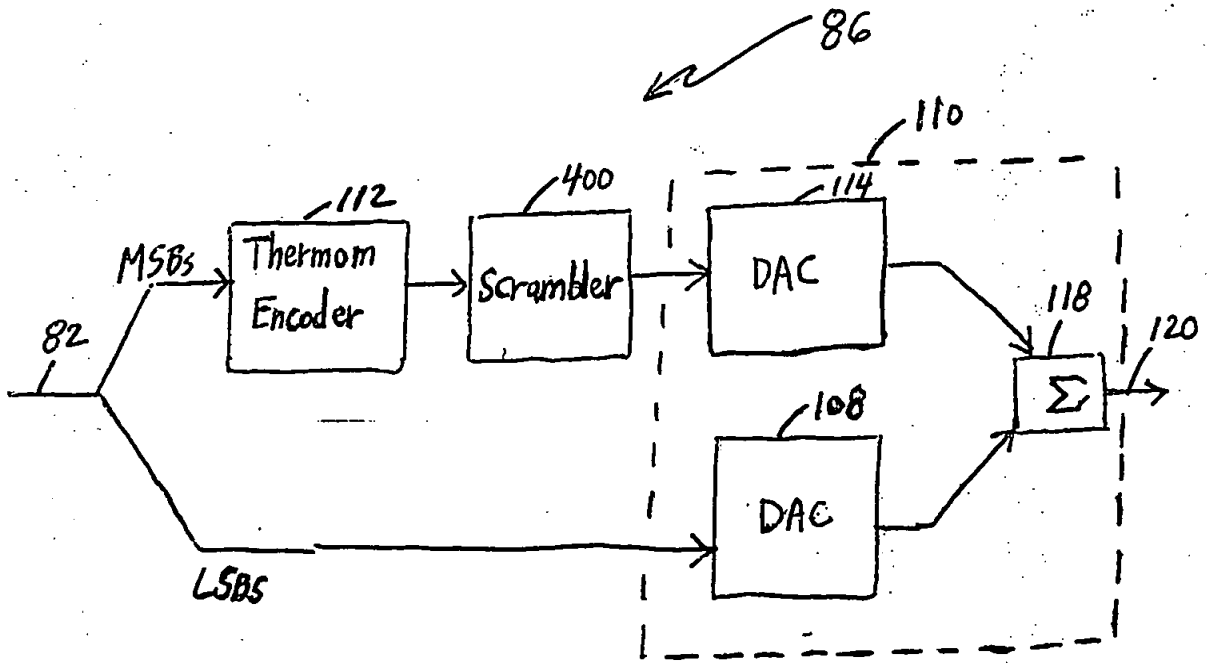

86
110
112
400
114
MSBs
Thermom Encoder
Scrambler
DAC
82
118
120
Σ
108
DAC
LSBs

FIG. 23

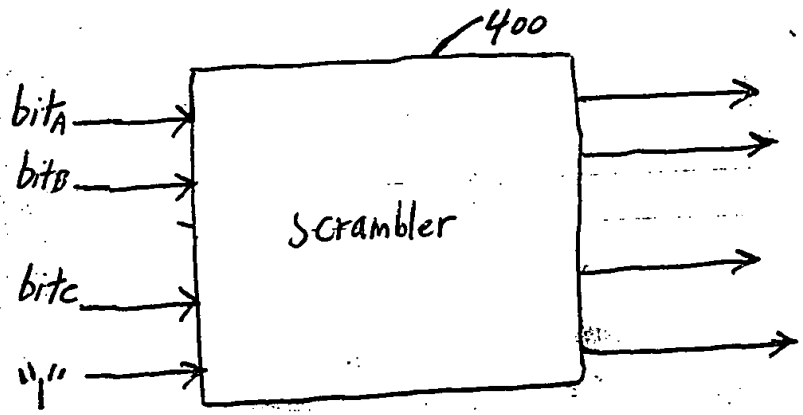



FIG 24

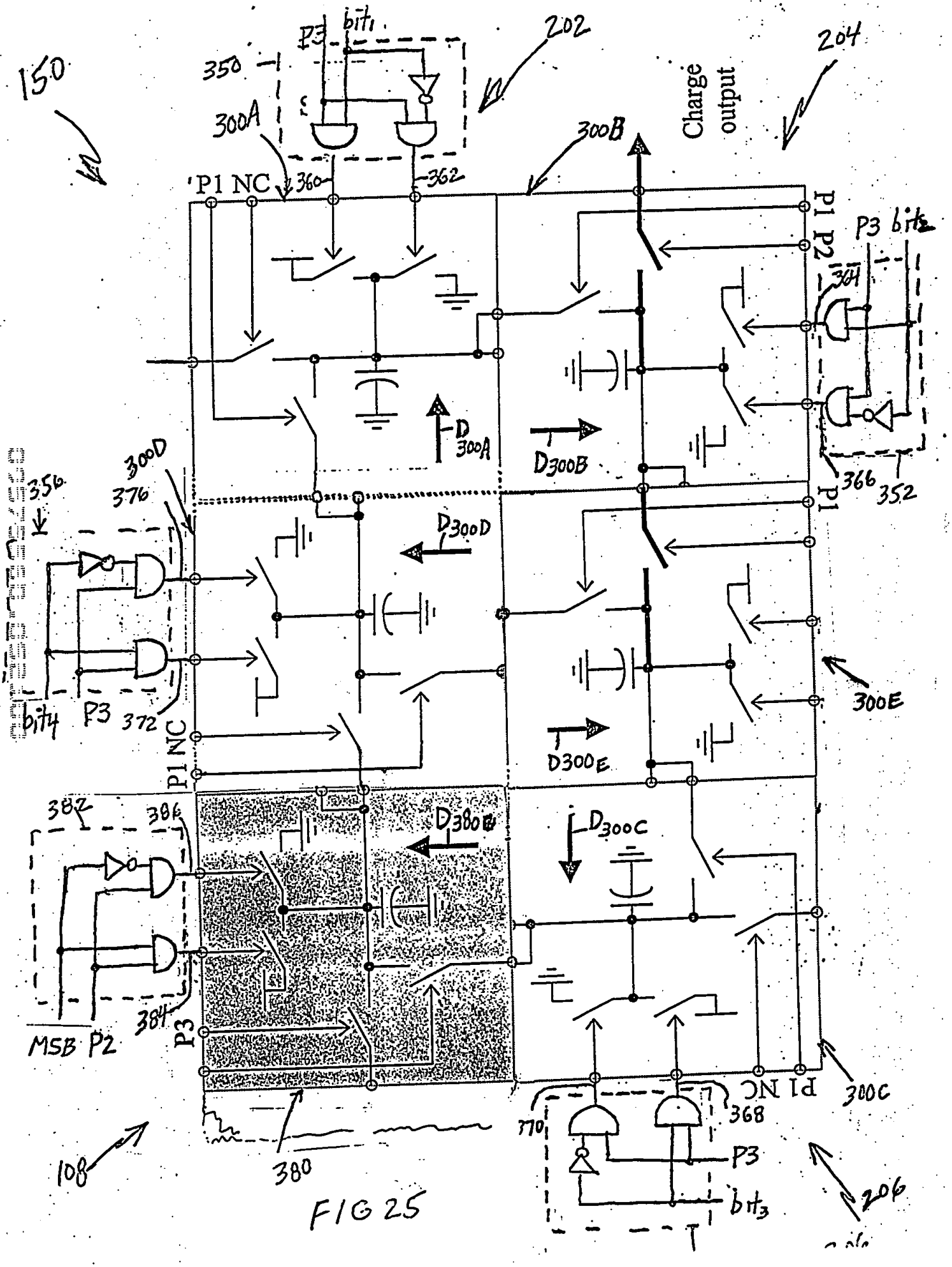

150
202
204
350
300A
300B
P3
bit1
Charge output
P1 NC
360
362
P1 P2
P3 bit2
384
366
352
P1
D300A
D300B
300D
376
356
D300D
bit4
P3
372
P1 NC
300E
D300E
382
386
D380B
D300C
MSB P2
384
P3
380
108
770
368
P3
bit3
206
300C
P1 NC

FIG 25

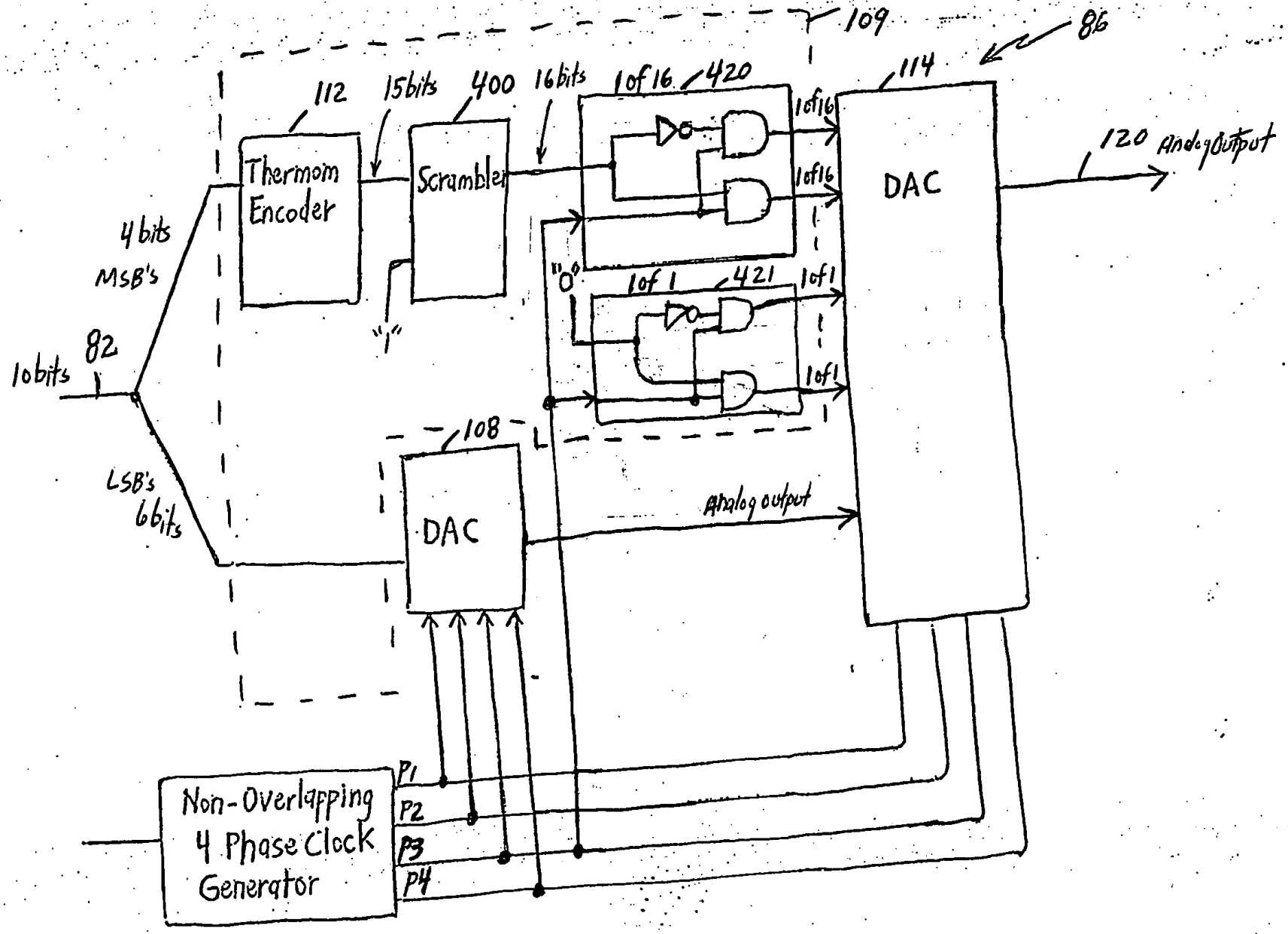

109
86
112
15bits
400
16bits
1of16
420
114
Thermom Encoder
Scrambler
1of16
1of16
DAC
120 Analog output
4 bits
MSB's
"0"
1of1
421
1of1
1of1
10bits
82
"1"
108
LSB's
6bits
DAC
Analog output
Non-Overlapping
4 Phase Clock
Generator
P1
P2
P3
P4

FIG 26

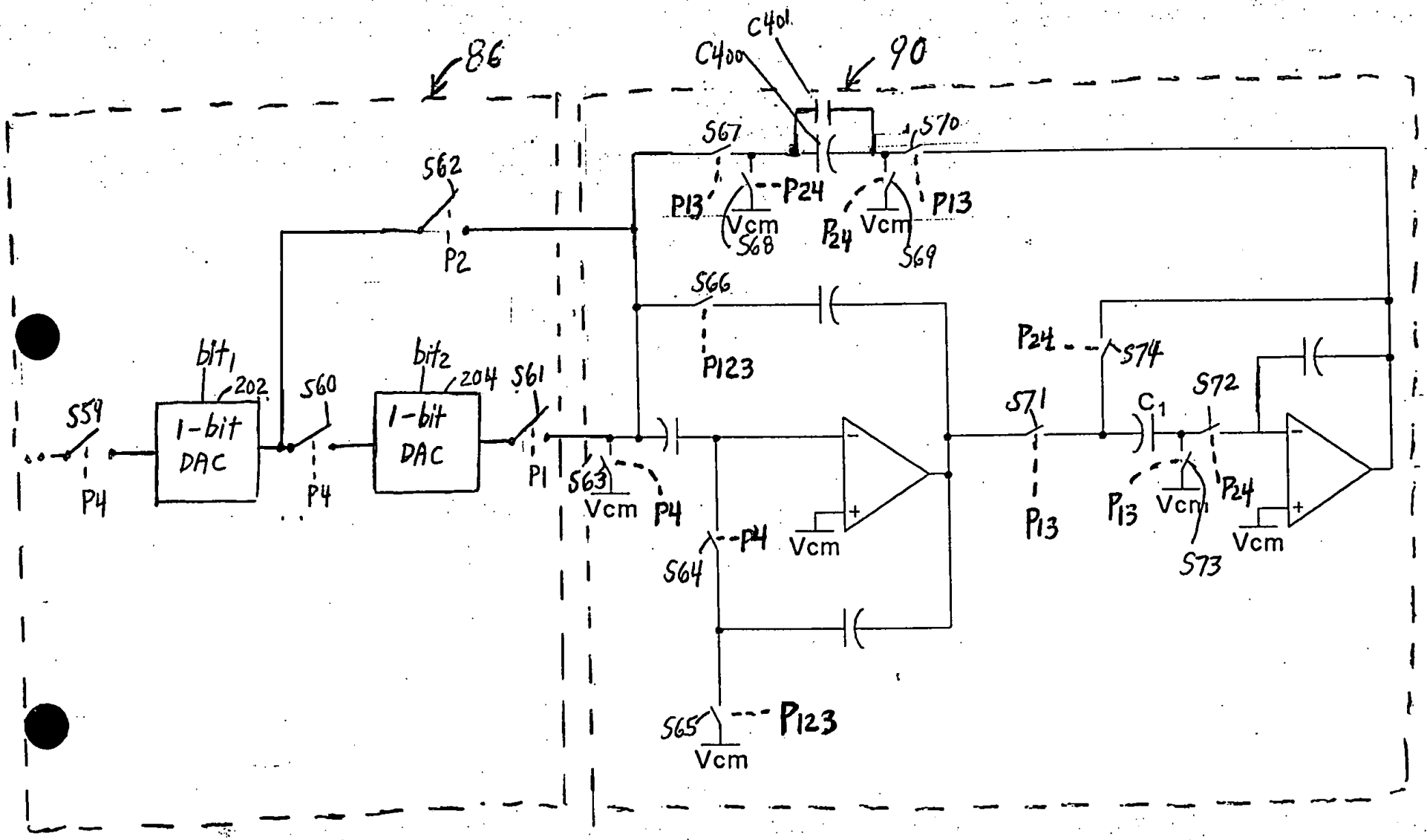

86
90
C400
C401
S67
S70
S62
P13
P24
Vcm
S68
S69
P2
S66
P123
bit1
202
bit2
204
S59
S60
S61
1-bit DAC
1-bit DAC
P4
P1
S63
S64
S65
P123
P24
S74
S71
S72
C1
P13
S73

FIG 27

FIG 28A

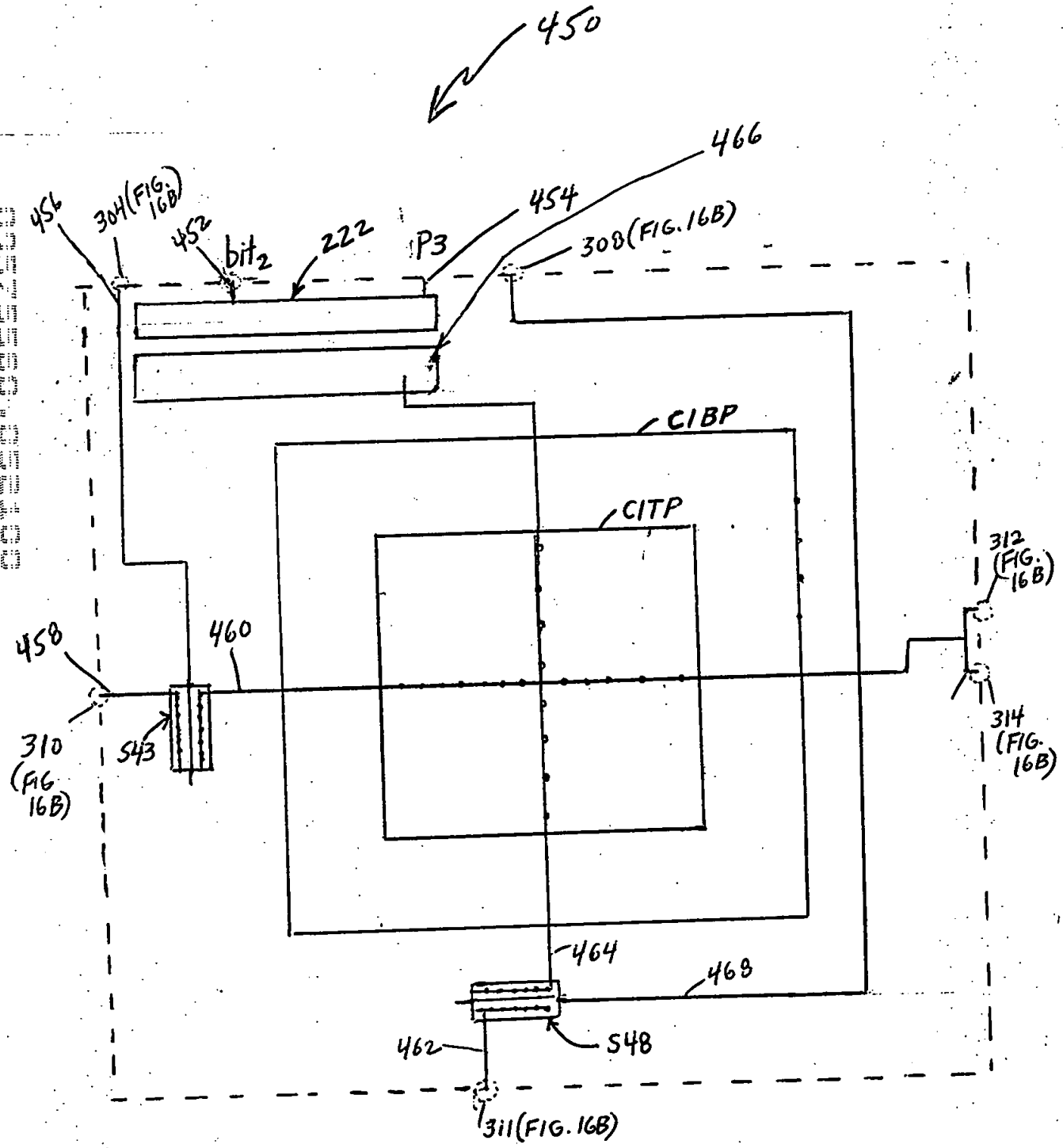
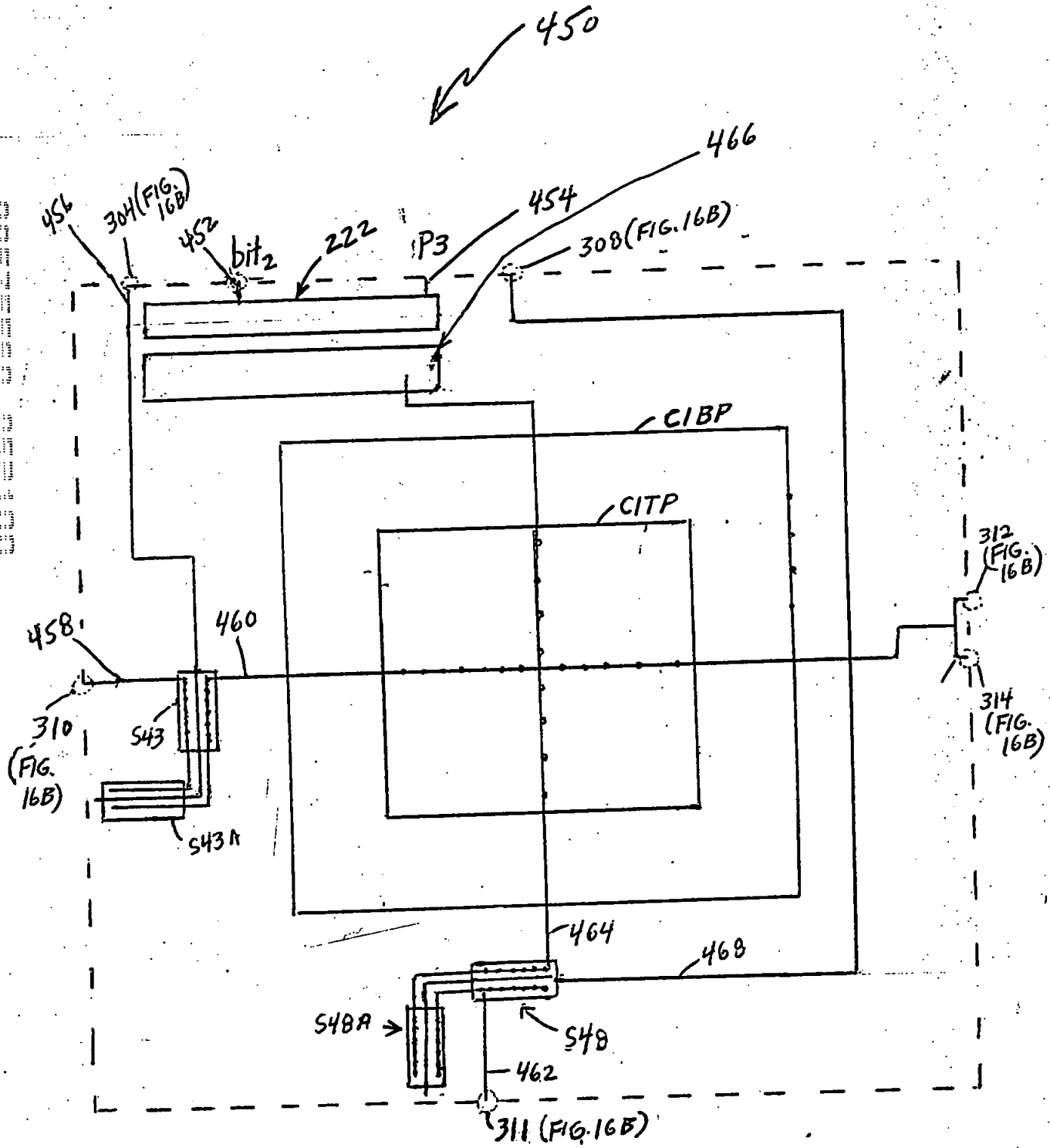

450
466
456
304(FIG. 16B)
452
bit2
222
P3
454
308(FIG. 16B)
CIBP
CITP
312 (FIG. 16B)
458
460
310 (FIG 16B)
543
314 (FIG. 16B)
464
468
462
548
311(FIG. 16B)

FIG 28B


450
466
456
304(FIG. 16B)
452
bit2
222
P3
454
308(FIG. 16B)
CIBP
CITP
312 (FIG. 16B)
458
460
310 (FIG. 16B)
S43
S43A
314 (FIG. 16B)
464
468
S48A
S48
462
311 (FIG. 16B)

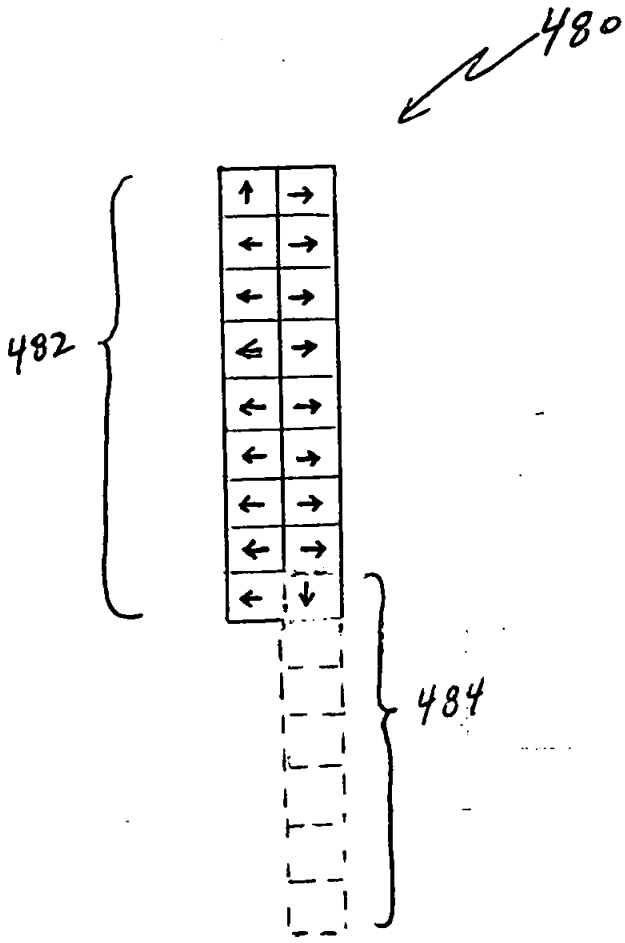



FIG. 29

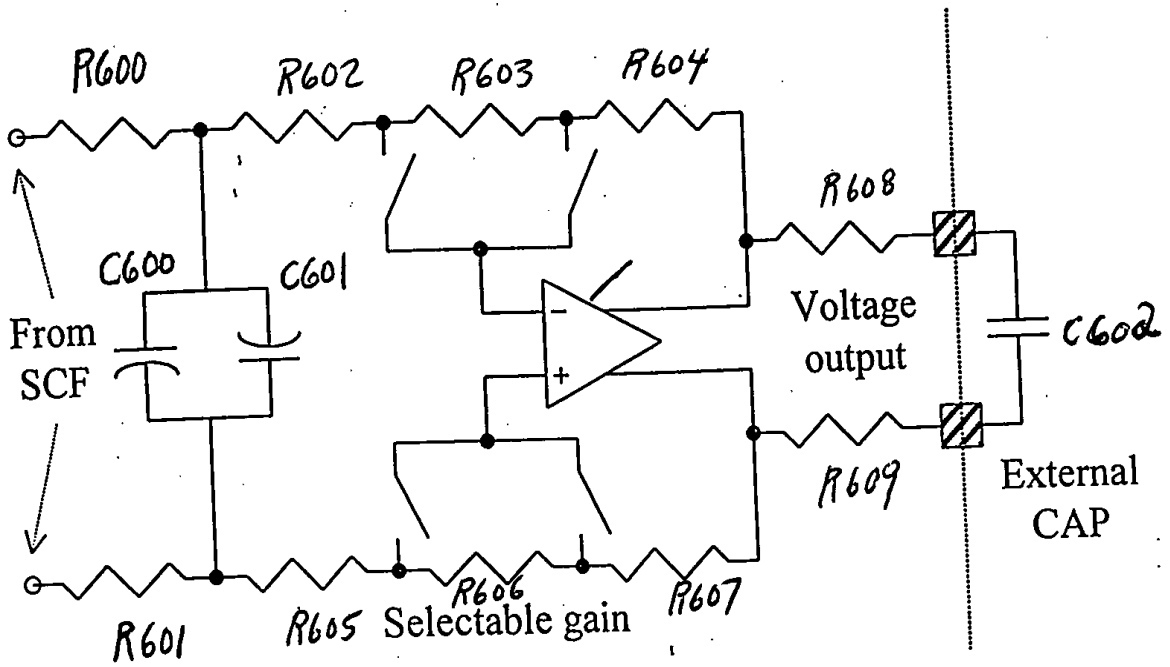

R600
R602
R603
R604
R608
C600
C601
From
SCF
Voltage
output
C602
External
CAP
R609
R601
R605
R606
Selectable gain
R607

FIG. 30

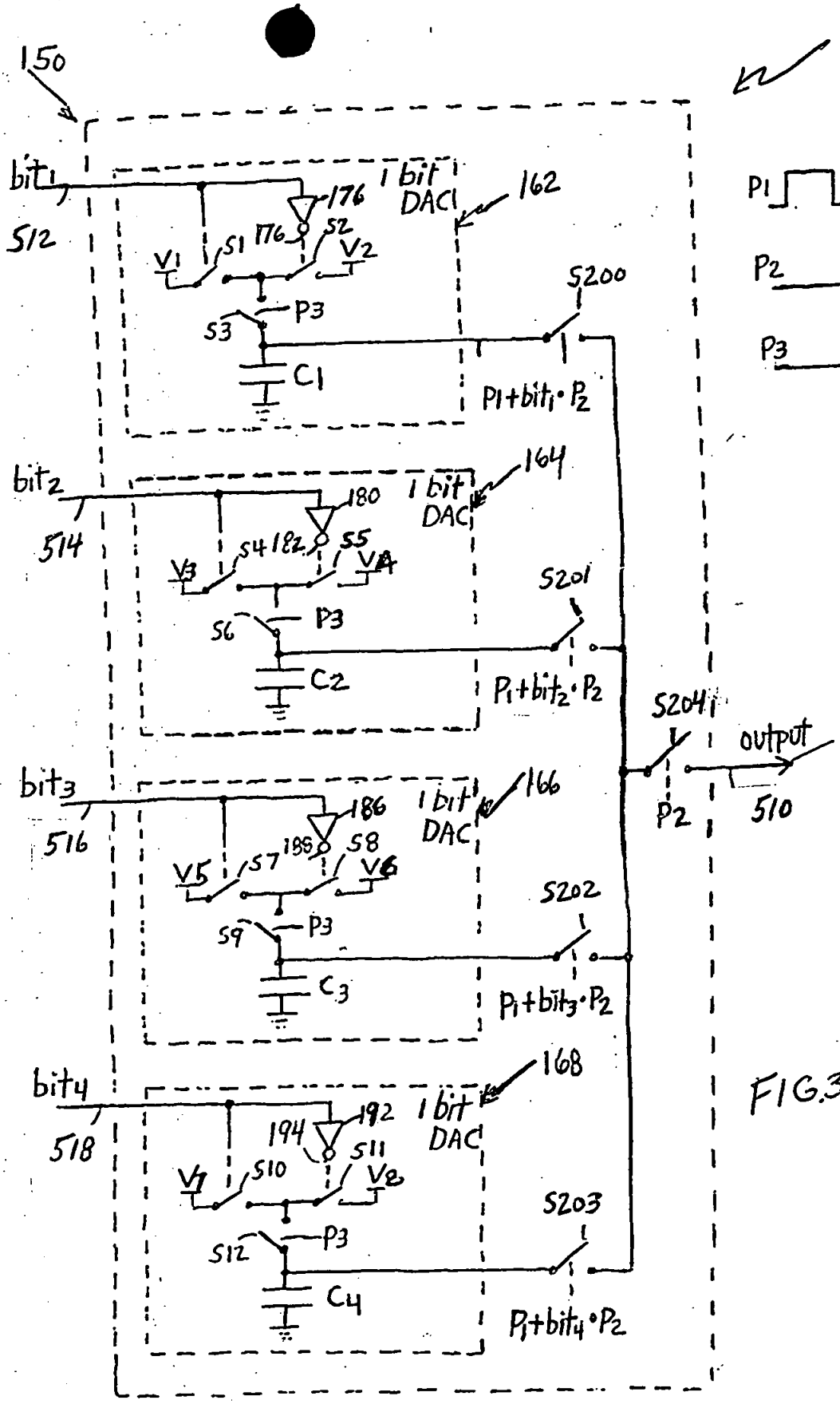

150
500
bit1
1 bit DAC
162
176
S1
S2
V1
V2
S12
P3
S3
C1
S200
P1+bit1·P2
bit2
1 bit DAC
164
180
S4
S5
182
V3
V4
514
S6
C2
S201
P1+bit2·P2
bit3
1 bit DAC
166
186
S7
S8
188
V5
V6
516
S9
C3
S202
P1+bit3·P2
bit4
1 bit DAC
168
192
194
S10
S11
V1
V2
518
S12
C4
S203
P1+bit4·P2
S204
output
P2
510

FIG.31

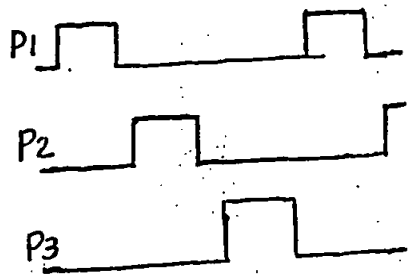

P1
P2
P3

FIG.32

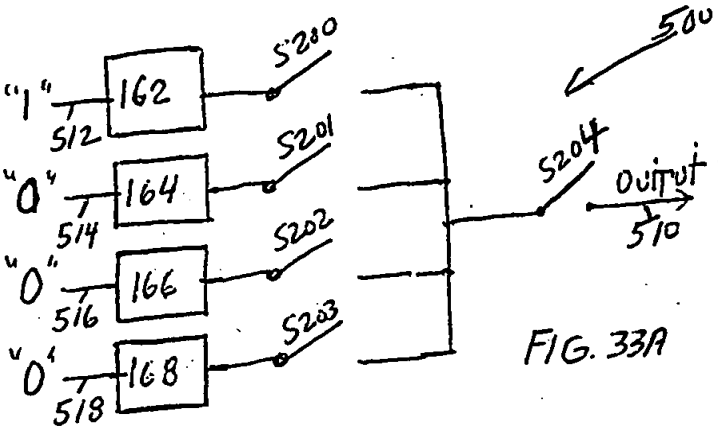



FIG. 33A

| | | |
|---|---|---|
| P1 "0" | $V(C_1) = V_{ref}$ | $Q(C_1) = C * V_{ref}$ |
| P2 "0" | $V(C_2) = 0$ | $Q(C_2) = 0$ |
| P3 "1" | $V(C_3) = 0$ | $Q(C_3) = 0$ |
| | $V(C_4) = 0$ | $Q(C_4) = 0$ |

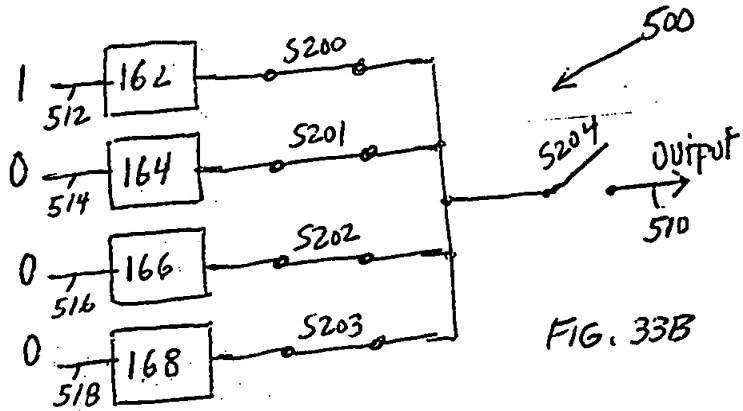



FIG. 33B

| | | |
|---|---|---|
| P1 = "1" | $V(C_1) = V_{ref}/4$ | $Q(C_1) = C * V_{ref}/4$ |
| P2 = "0" | $V(C_2) = V_{ref}/4$ | $Q(C_2) = C * V_{ref}/4$ |
| P3 = "0" | $V(C_3) = V_{ref}/4$ | $Q(C_3) = C * V_{ref}/4$ |
| | $V(C_4) = V_{ref}/4$ | $Q(C_4) = C * V_{ref}/4$ |

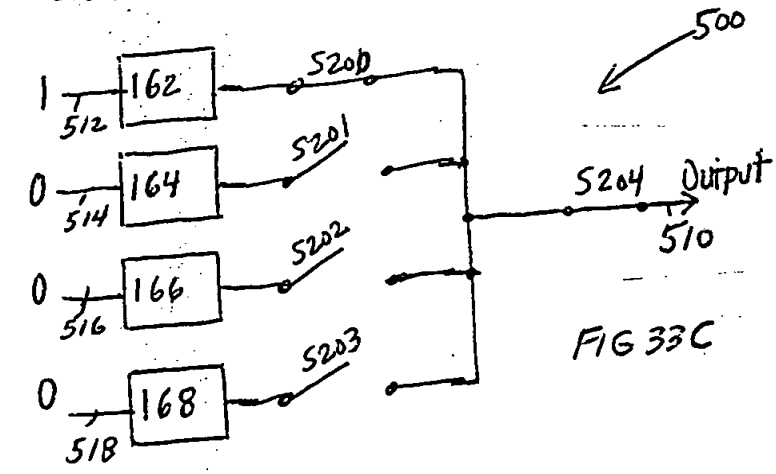



FIG 33C

| | | |
|---|---|---|
| P1 = "0" | $V(C_1) = V_{ref}/4$ | $Q(C_1) = C * V_{ref}/4$ |
| P2 = "1" | $V(C_2) = V_{ref}/4$ | $Q(C_2) = C * V_{ref}/4$ |
| P3 = "0" | $V(C_3) = V_{ref}/4$ | $Q(C_3) = C * V_{ref}/4$ |
| | $V(C_4) = V_{ref}/4$ | $Q(C_4) = C * V_{ref}/4$ |

Q delivered to output terminal is $Q(C_1) = C * V_{ref}/4$

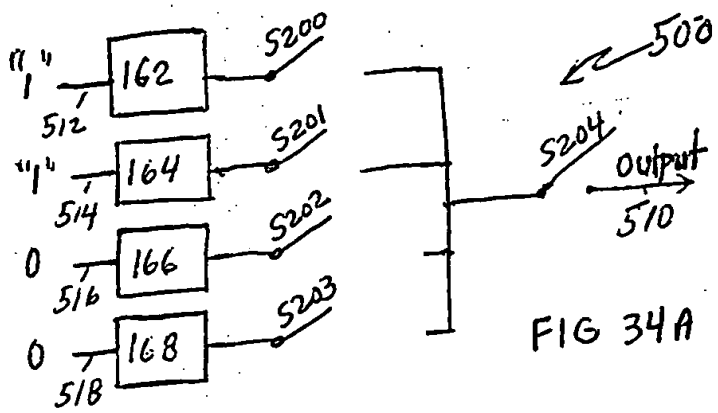



FIG 34A

| | | |
|---|---|---|
| P1 "0" | $V(C_1) = V_{ref}$ | $Q(C_1) = C * V_{ref}$ |
| P2 "0" | $V(C_2) = V_{ref}$ | $Q(C_2) = C * V_{ref}$ |
| P3 "1" | $V(C_3) = 0$ | $Q(C_3) = 0$ |
| | $V(C_4) = 0$ | $Q(C_4) = 0$ |

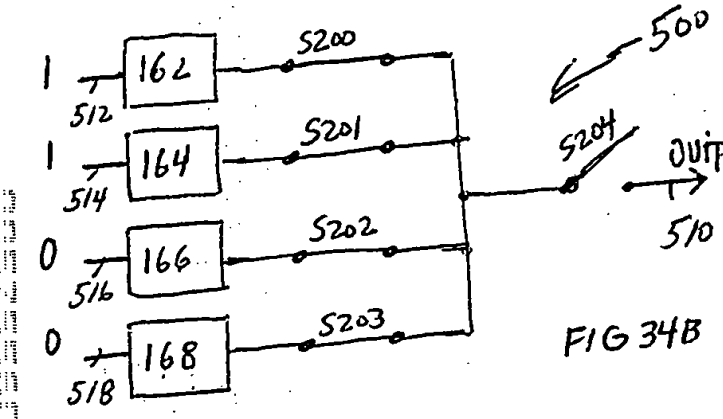



FIG 34B

| | | |
|---|---|---|
| P1 = "1" | $V(C_1) = V_{ref}/2$ | $Q(C_1) = C * V_{ref}/2$ |
| P2 = "0" | $V(C_2) = V_{ref}/2$ | $Q(C_2) = C * V_{ref}/2$ |
| P3 = "0" | $V(C_3) = V_{ref}/2$ | $Q(C_3) = C * V_{ref}/2$ |
| | $V(C_4) = V_{ref}/2$ | $Q(C_4) = C * V_{ref}/2$ |

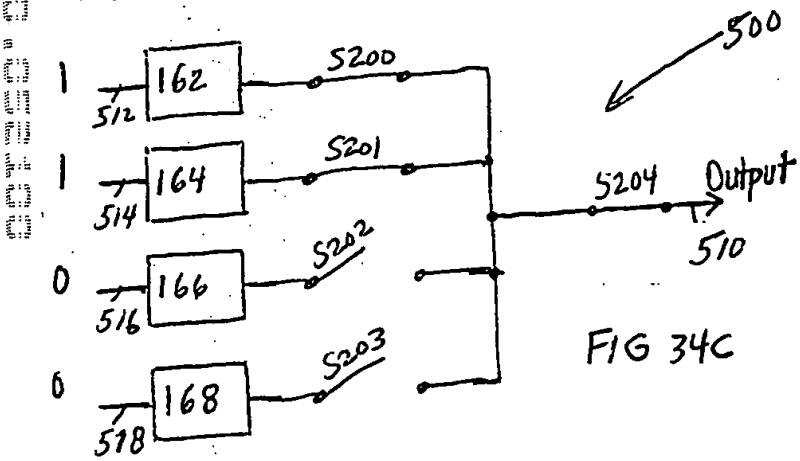



FIG 34C

| | | |
|---|---|---|
| P1 = "0" | $V(C_1) = V_{ref}/2$ | $Q(C_1) = C * V_{ref}/2$ |
| P2 = "1" | $V(C_2) = V_{ref}/2$ | $Q(C_2) = C * V_{ref}/2$ |
| P3 = "0" | $V(C_3) = V_{ref}/2$ | $Q(C_3) = C * V_{ref}/2$ |
| | $V(C_4) = V_{ref}/2$ | $Q(C_4) = C * V_{ref}/2$ |

Q delivered to output terminal is $Q(C_1) + Q(C_2) =$

$C * V_{ref}/2 + C * V_{ref}/2 =$

$C * V_{ref}$

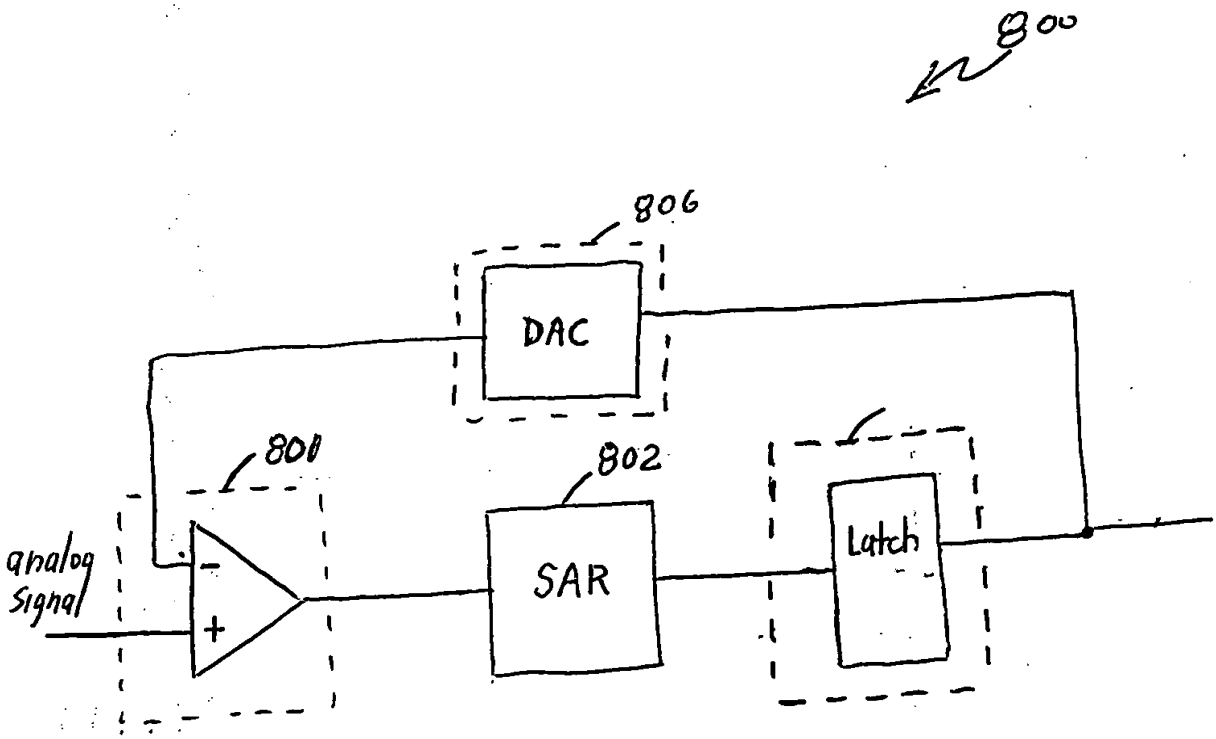



FIG. 35